

# 10<sup>th</sup> European Heterostructure Technology Workshop

September 18 - 19, 2000

University of Ulm  
International Institute Schloss Reisensburg  
Günzburg, Germany

LATE POSTER SUBMISSIONS

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# 10th European Heterostructure Technology Workshop

## Poster Session

Monday, 18.09.00

17:30 - 19:00

**M. Myronov, C.P. Parry, O.A. Mironov, E.H.C. Parker and T.E. Whall**  
Post-Growth Annealing Effect on Magneto-Transport and Structural Properties  
of  $\text{Si}_{0.2}\text{Ge}/\text{Si}_{0.65}\text{Ge}_{0.35}/\text{Si}(001)$  Modulation Doped Heterostructure  
Univ. of Warwick, Dept. of Physics, United Kingdom

**M. Kunze\*, F. Banhart\*\*, E. Kohn\***  
Growth and Characterization of Low Temperatures  
Grown Inp on Foreign Substrates  
Univ. of Ulm, Germany      \*Dept. of Electron Devices & Circuits  
\*\*Dept. of Electron Microscopy

**M. Neuburger\*, I. Daumiller\*, P. Schmid\*, E. Kohn\***  
**C. Kirchner\*\*, M. Seyboth\*\*, M. Kamp\*\***  
Device Simulation and Characterization of GaN/InGaN/GaN Heterostructure FET  
Univ. of Ulm, \*Dept. of Electron Devices & Circuits, Germany  
\*\*Dept. of Optoelectronics

**R. Müller, M. Adamschik, A. Denisenko, E. Kohn**  
Diamond pH-Sensor  
Univ. of Ulm, Dept. of Electron Devices & Circuits, Germany

**Y. Guhel, B. Boudart, T. Heim, N. Grandjean\*, F. Omnes\*, J.C. De Jaeger**  
Dry etching for gate recessing on AlGaIn/GaN HEMT's  
IEMN, Lille, France

**J. Bendedikt, Paul J. Tasker**  
High Power Time Domain Measurement System with Active Harmonic  
Load-Pull for Base Station Amplifier Design  
Cardiff University, Cardiff, United Kingdom

**M. Lagadas\*, A. Müller\*\*, G. Konstantinidis\*, G. Deligeorgis\*, S. Iordanescu\*\*,  
I. Petrini\*\*, D. Vasilache\*\*, P. Blondy\*\*\***  
Low Temperature GaAs Micromachined Membranes as Support for MMIC  
Passive Elements  
\* Forth IESL, Heraklion, \*\* IMT Bucharest, \*\*\*IRCOM Limoges

**S. Kiatgamolchai, M. Myronov, O.A. Mironov, E.H.C. Parker, T.E. Whall**  
A Novel Mobility Spectrum Maximum Entropy Approach for Magnetotransport  
Analysis of SiGe/Si Heterostructures  
Univ. of Warwick, Dept. of Physics, Coventry, UK

**V. Ziegler\*, C. Woelk\*, R. Deufel\*, F. Berlec\*, J. Dickmann\***  
**C. Gaessler\*\*, N. Käß\*\*, E. Kohn\*\*, H. Schumacher\*\***  
InP-Based and GaAs-Metamorphic Devices for Multifunctional mm-Wave Applications  
\*DaimlerChrysler AG, Research Center Ulm, Germany  
\*\*Univ. of Ulm, Dept. of Electron Devices & Circuits, Germany

# Growth and Characterization of Low Temperature Grown InP on Foreign Substrates

M. Kunze, F. Banhart\* and E. Kohn

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\*Department of Electron Microscopy, University of Ulm, D-89069 Ulm, Germany

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An approach to overcome limitations in poly-Si or Polymer TFT-devices caused by low carrier mobilities in the range of a few  $10 \text{ cm}^2/\text{Vs}$  would be merging low cost substrates with the high performance III/V technologies. Several technologies, e.g. epitaxial lift-off, are used for replacement of expensive substrates. However, for direct deposition only a limited temperature range is available due to the limited thermal stability of most substrates. But doping at low growth temperatures is difficult due to deviation from the ideal stoichiometry of III/V materials grown below  $350^\circ\text{C}$  caused by incorporated excess As and P respectively in the lattice. In the case of InP grown at low temperatures (LTG-InP) excess P appears partially as antisite on In sites. The first excited state of the P-antisites lies 250 meV above the conduction band edge and therefore leads to auto-doped n-type layers. This technology leads to carrier concentrations and mobilities comparable to conventionally grown and Si-doped samples on InP-substrates [1]. This presentation aims at the replacement of InP-substrates through low cost temperature sensitive substrates to be used in the low GHz regime for example in low cost wireless receiver chips on polymers (plastic tags). The presented structure consists of a basic LTG-GaAs/LTG-InP/LTG-GaAs heterostructure (see Fig. 2, left) using LTG-GaAs as buffer and gate barrier layer [2]. Transferring the LTG-InP active layers onto foreign substrates the carrier mobility drops with increasing effective lattice mismatch and defect density. However, the range of the carrier mobility remains still at high values on different substrates: a) InP  $\mu \approx 2000 \text{ cm}^2/\text{Vs}$ , b) GaAs  $\mu \approx 500 \text{ cm}^2/\text{Vs}$ , c) Si  $\mu \approx 500 \text{ cm}^2/\text{Vs}$  and d) Sapphire  $\mu \approx 200 \text{ cm}^2/\text{Vs}$  [3]. On GaAs and Si substrates TEM-, AFM- and HRXRD-analysis revealed still crystalline structures however with extremely high defect densities (Fig.1). In the FET device, besides the channel mobility and channel sheet charge, gate and buffer leakage are important. Especially low surface roughness and interface leakage currents require specific optimization of the growth process to control for example the P and As surplus concentration generated by the low temperature growth. On GaAs with a highly disordered layer stack as shown in Fig.2 (left) this optimization has, for the first time, already lead to fully functional output characteristics as shown in Fig.2 (right). For a gate length of  $l_g = 1.5 \mu\text{m}$  an  $f_t = 1.2 \text{ GHz}$  and  $f_{max} = 2.4 \text{ GHz}$  were obtained. LTG-InP based FETs on Si substrate could be fabricated (Fig.3) using a back gate device configuration. Due to the large surface roughness (Fig.1 (right)) in FETs with top gate the channel charge could not be modulated. First results on and polycrystalline Si will be discussed.

## REFERENCES

- [1] B. Henle and E. Kohn, "InP based HFET structure grown and processed at very low temperatures below  $300^\circ\text{C}$ ," *55th Annual Device Research Conference Digest*, pp. 74-75, June 1997.
- [2] L.H. Lee, M. Kunze, B. Henle, and E. Kohn, "HF Characteristics of InP-Based HFETs Grown at Extremely Low Temperatures of  $300^\circ\text{C}$  and Below," *Proceedings IPRM 98, University of Tsukuba, Ibaraki, Japan*, pp. 513-516, May 1998.
- [3] M. Kunze, L.H. Lee, H.Y. Chung, and E. Kohn, "Demonstration of Low Temperature Grown InP-channel HFET transferred onto GaAs substrate," *Solid-State Electronics*, vol. 43, pp. 1535-1540, 1999.

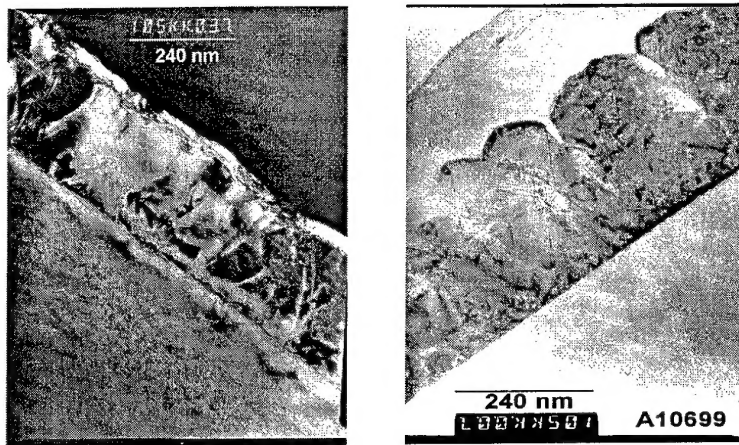


Fig. 1. TEM photograph of LTG-InP FET heterostructure on GaAs substrate (left) and a heterostructure on Si-Substrate for mobility analysis (right)

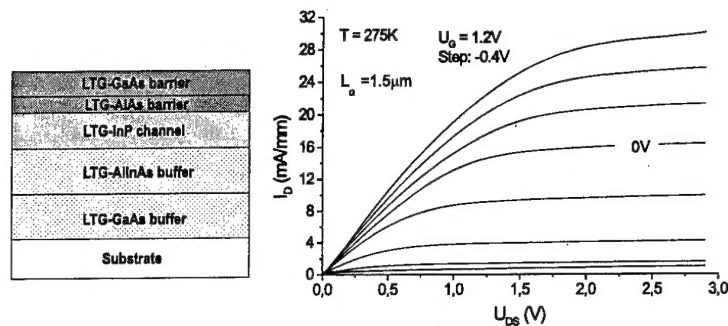


Fig. 2. Schematic device structure (left) and DC output characteristics of LTG-InP FET heterostructure on GaAs substrate shown in fig. 1 left side

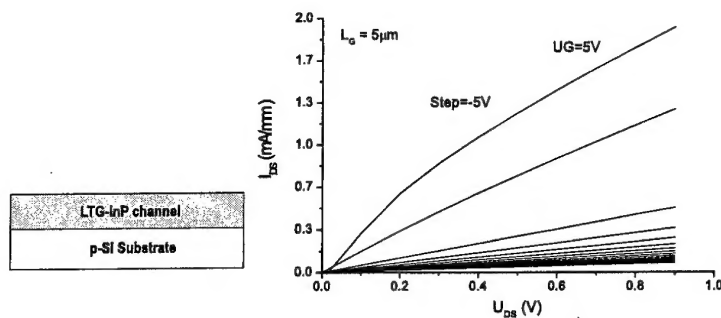


Fig. 3. Schematic device structure (left) and DC output characteristics of LTG-InP FET on Si substrate

## Device Simulation and Characterization of GaN/InGaN/GaN Heterostructure FET

M. Neuburger, I. Daumiller, P. Schmid, and E. Kohn

Dept. of Electron Devices and Circuits, University of Ulm, 89069 Ulm, Germany

C. Kirchner, M. Seyboth, M. Kamp

Department of Optoelectronics, University of Ulm, 89069 Ulm, Germany

GaN is the only widely used highly polarized electronic wide bandgap material up to now. Including ternary heterostructures like AlGaIn/GaN, the stress generates an additional spontaneous polarization. Both spontaneous and piezo-electric polarization induce piezo-charges at the surfaces and interfaces. The induced charge is a dipole charge by nature requiring charge neutrality. In case of an electronic piezo-charge in the channel, like in the case of the piezo-FET, the counter charge must be located on the surface. This charge may be molecular or electronic and may reside in a surface state. Thus, it is not obvious how equilibrium is reached in this case and the device may suffer from instabilities in its characteristics [1].

Instead, in a GaN/InGaIn/GaN FET structure the piezo-induced charges are located at the GaN/InGaIn interfaces not involving the surface (figure 1). Theoretically higher mobilities and higher strain induced piezo-charges in the InGaIn channel are additional advantages.

To obtain a GaN/InGaIn/GaN HFET device consisting only of an electron channel, it is necessary to compensate the positive piezo-induced charge by a fixed donor charge. This donor charge may be realized by backside n-doping of the InGaIn channel (figure 2) or by backside modulation doping like in the case of an inverted HEMT structure (figure 3).

Such novel structures have been simulated using the Silvaco device simulator (figure 4 & 5). For simulation a piezo-charge model has been implemented using data available for strained InGaIn [2]. The sheet charge is simulated by using delta doping profiles.

To verify the simulated results, first GaN/InGaIn/GaN HFETs with backside doping of the InGaIn channel have been fabricated yielding current densities of 240mA/mm (figure 6).

[1] E. Kohn, I. Daumiller, P. Schmid, N. X. Nguyen, C.N. Nguyen, "Large signal frequency dispersion of AlGaIn/GaN heterostructure field effect transistors", Electronic Letters, Vol. 35 (1999)

[2] O. Ambacher, "Growth and applications of Group III-nitrides", J. Phys. D: Appl. Phys. 31 (1998) 2653-2710

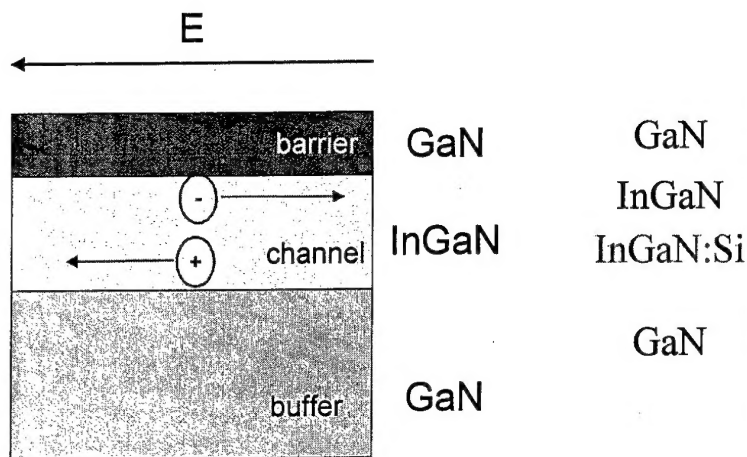


Figure 1: GaN/InGaN/GaN-FET structure

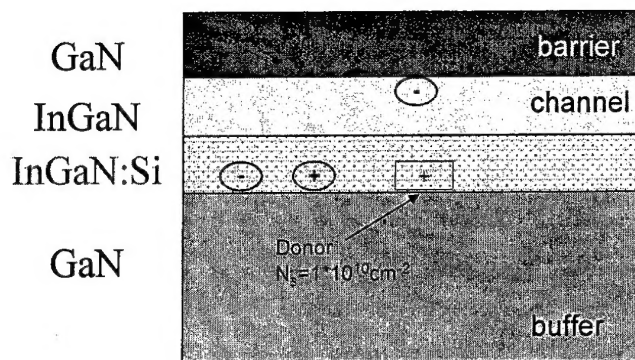


Figure 2: Backside n-doped InGaN channel

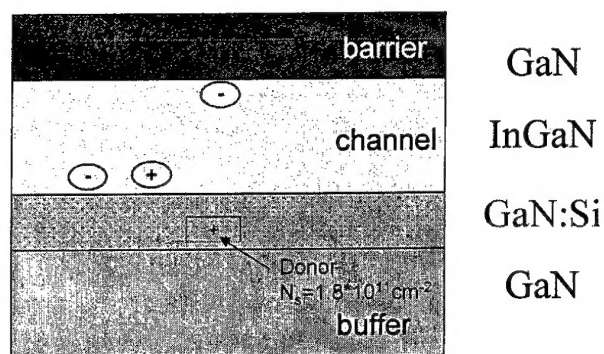


Figure 3: Inverted HEMT structure

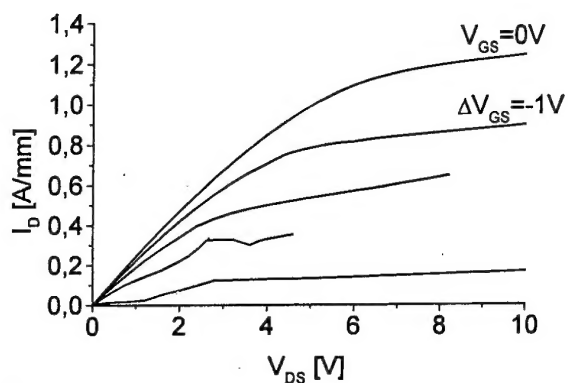


Figure 4: Simulated DC-output of figure 3

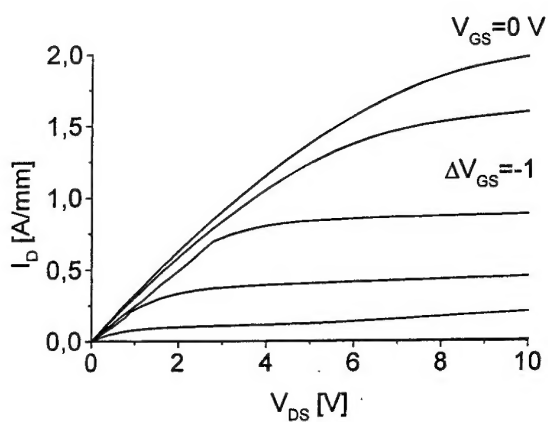


Figure 5: Simulated DC-output of figure 2

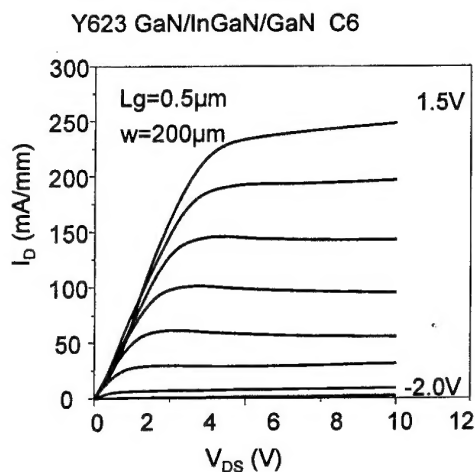


Figure 6: Measured DC-output

# InP-based and GaAs-metamorphic devices for multifunctional mm-wave applications

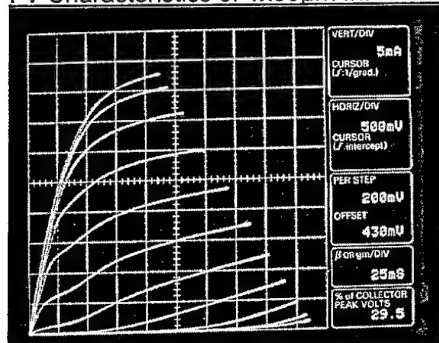
Volker Ziegler, Claus Wölk, Reinhard Deufel, Franz-Josef Berlec, Jürgen Dickmann  
DaimlerChrysler AG, Research Center Ulm, Wilhelm-Runge-Straße 11, D-89081 Ulm, Germany  
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Christoph Gässler, Norbert Käß, Erhard Kohn, Hermann Schumacher  
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Albert-Einstein-Allee 45, D-89081 Ulm, Germany  
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## Abstract:

On this poster we present our InP-based and GaAs-metamorphic devices for multifunctional mm-wave applications. InP and GaAs-metamorphic PIN-Diodes, HFETs for low noise and power applications are compared. The poster shows that very high performance devices can be realized either on InP or GaAs-metamorphic substrates. The devices show comparable DC and RF-performance. The metamorphic buffers have been investigated to get a very high relaxation of 94% in lattice constant. Coplanar mm-wave circuits have been realized using this devices and are finally combined in a multifunctional MMIC including a switch and a low noise amplifier.

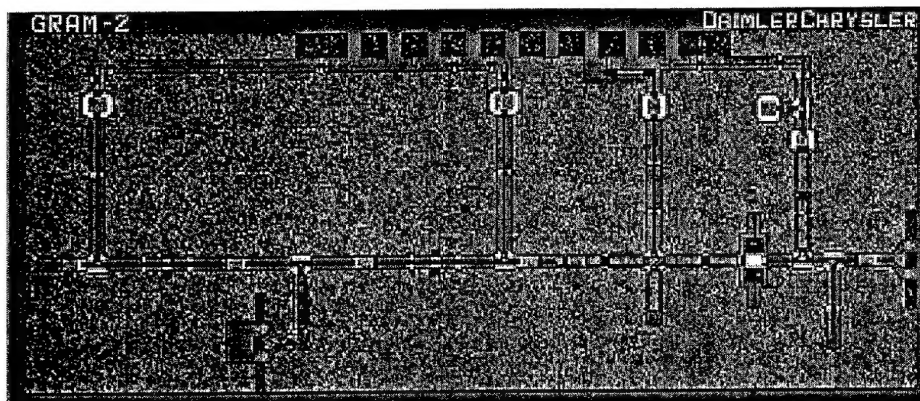
## I-V Characteristics of 1x60µm InP Power-HFET



## DC- and RF-Performance of the Power HFET-devices

$R_{SH}$ [Ohm/square]	$g_{max}$ [mS/mm] @ $V_{GS}$ [V], $V_{DS}=2.5V$	$I_{DS}$ @ $g_{max}$ [mA/mm]	$I_{DS,max}$ @ $V_{DS}=2.5V$	$V_{GD,breakdown}$ @ 1mA/mm	$P_{out,max}$ [mW/mm] @ 12GHz
134	610 @ -0.3V	380	700	-4.9 V	645

## Multifunctional heterointegrated MMIC including SPDT switch and LNA





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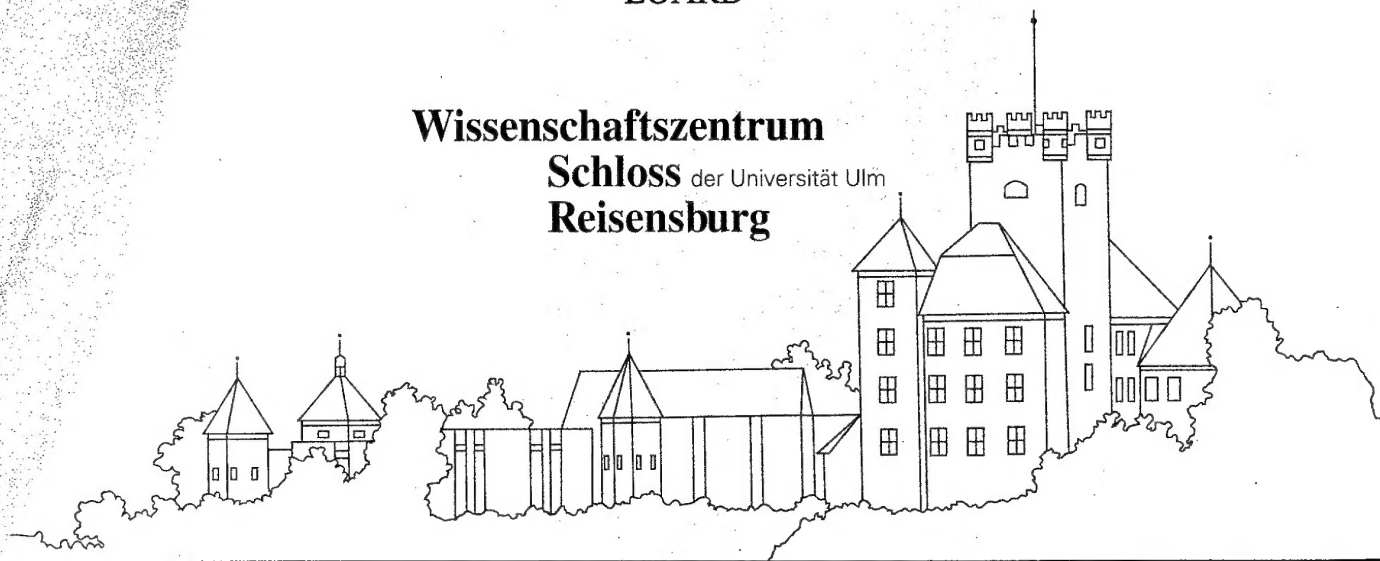
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# PROGRAMME

# 10th European Heterostructure Technology Workshop

**Monday, 18.09.00**

## **Session B** **SiGe devices**

- 11:15-11:30     **J. Kuchenbecker<sup>1</sup>, M. Borgarino<sup>2</sup>, L. Bary<sup>1</sup>, J.G. Tartarin<sup>(1)(4)</sup>, Kovacic<sup>(3)</sup>, Lafontaine<sup>(3)</sup>, R. Plana<sup>(1)(4)</sup>, F. Fantini<sup>(2)</sup>, J. Graffeuil<sup>(1)(4)</sup>**  
Investigation of Hot Carrier Induced Degradations in Microwave SiGe HBTs  
<sup>(1)</sup> LAAS-CNRS, Toulouse, France  
<sup>(2)</sup> Univ. of Modena and Reggio Emilia, Modena, Italy  
<sup>(3)</sup> SiGe Microsystem, Canada; <sup>(4)</sup> University Paul Sabatier, Toulouse, France
- 11:30-11:45     **M. Myronov, E.H.C. Parker, T.E. Whall, S.G. Lyapin, P.C. Klipstein**  
Thermal Annealing Effect on Properties of  $\text{Si}_{0.2}\text{Ge}_{0.8}/\text{Si}_{0.7}\text{Ge}_{0.3}/\text{Si}(001)$  p-Type Modulation  
Univ. of Warwick, Dept. of Physics, UK
- 11:45-12:00     **M. Prest\*, G. Braithwaite, T. Grasby, P. Phillips, B.K. Jones<sup>1</sup>, E.H.C. Parker, T.E. Whall**  
Low Frequency Noise in  $\text{Si}/\text{Si}_{1-x}\text{Ge}_x/\text{Si}$  Heterostructure p-Channel MOSFETs  
Univ. of Warwick, Dept. of Physics, UK; Univ. of Lancaster, <sup>1</sup>Dep. Of Physics, UK
- 12:00-12:15     **G. Hoeck, T. Hackbarth\*, M. Myronov\*\*, O.A. Mironov\*\*, E.H.C. Parker\*\*, E. Kohn**  
Magneto-transport properties of  $\text{Si}_{1-x}\text{Ge}_x/\text{Si}_{1-y}\text{Ge}_y/\text{Si}(001)$   
Univ. of Ulm, Dept. of Electron Devices and Circuits, Ulm, Germany  
\*Daimler Chrysler AG, Ulm  
\*\*Univ. of Warwick, Dept. of Physics, Coventry, UK
- 12:15-14:00     LUNCH

## **Session C** **Emerging Technologies**

- 14:00-14:30     **D. Vuillaume (invited)**  
Organic Devices at Nanometer Scale Using Self-Assembled Monolayers  
IEMN, Lille, France
- 14:30-15:00     **H. Klauk (invited)**  
Organic TFTs and Integrated Circuits  
Infineon, Dept. MP PMT, Erlangen, Germany
- 15:00-15:30     BREAK

# 10th European Heterostructure Technology Workshop

**Monday, 18.09.00**

**8:00-8:15      Welcome**

## **Session A**

### **A1 III V Nitride - Materials growth**

- 8:15-8:45      O. Ambacher (invited)**  
Polarization Induced Effects in Group-III-Nitride Heterostructures and Devices  
WSI, TU Munich, Germany
- 8:45-9:00      M. Seyboth, C. Kirchner, M. Scherer, V. Schwegler, M. Kamp**  
MOCVD Growth of III-V Nitrides for Electronic Applications:  
Problems and Special Features  
Univ. Ulm, Dept. of Optoelectronics, Ulm, Germany
- 9:00-9:15      M. Scherer, M. Seyboth, V. Schwegler, M. Kamp**  
Dry Etching Influence on Contact Formation to Gallium Nitride  
Univ. of Ulm, Dept. of Optoelectronics, Ulm, Germany
- 9:15-9:30      S. Mikroulis<sup>1</sup>, A. Georgakilas<sup>1</sup>, G. Constantinidis<sup>1</sup>, K. Amimer<sup>1</sup>, V. Cimalla<sup>1</sup>, A. Kostopoulos<sup>1</sup>,  
E. Dimakis<sup>1</sup>, M. Androulidaki<sup>1</sup>, E.-M. Pavelescu<sup>1</sup>, K. Tsagaraki<sup>1</sup>, Z. Hatzopoulos<sup>1</sup>  
and V. Yu. Davidov<sup>2</sup>**  
Growth Dependent Properties of GaN on Al<sub>2</sub>O<sub>3</sub>(0001) Grown by Radio Frequency  
Plasma-Assisted Molecular Beam Epitaxy  
<sup>1</sup> Forth/IESL and Univ. Crete, Physics Dept., Microelectronics Research Group  
<sup>2</sup> Ioffe Physico-Technical Inst., St. Petersburg, Russia
- 9:30-9:45      A. Wiesz, J.-S. Lee, R. Dietrich, A. Vescan, H. Leier**  
AlGaIn/GaN FETs: Performance and Problems  
DaimlerChrysler AG, Ulm
- 9:45-10:15      BREAK**

### **A2 Diamond growth**

- 10:15-10:30      K. Janischowsky, M. Stammer, F. Maier, L. Ley**  
Growth of Oriented Diamond Thin Films on Si (100) with Semiconductor Quality  
Univ. of Ulm, Dept. of Elec. Dev. & Circuits and Univ. Erlangen, Inst. for Tech. Physics, Germany
- 10:30-10:45      Alexander Kromka, V. Malcher, V. Dubravcová, A. Satka**  
Electron Assisted Hot-Filament CVD Deposition of Diamond Films  
Slovak Univ. of Technology, Dept. of Microelectronics, Ilkovicova, Bratislava
- 10:45-11:00      Viliam Malcher, Alexander Kromka, Ján Janík, Viera Dubravcová**  
Temperature Dependence of Quality for Diamond Thin Films Deposited on  
Si (100) Via Double Bias-Assisted HFCVD  
Slovak Univ. of Technology, Dept. of Microelectronics, Bratislava
- 11:00-11:15      BREAK**

# 10th European Heterostructure Technology Workshop

Monday, 18.09.00

## Session D

### D1 III V - Sensors

- 15:30 - 16:00     **A. Schlachetzki (Invited)**  
Micro-electromechanical systems  
Techn. Univ. Braunschweig, Inst. für Halbleitertechnik, Germany
- 16:00 - 16:15     **Idris Akar, K. Mutamba, C. Euterneck, H. Aarab, S. Coulibaly, S. Brecht, H.L. Hartnagel**  
Technology of Integrated Application Specific GaAs Flow Sensors  
Techn. Univ. Darmstadt, Inst. f. Hochfrequenztechnik, Germany
- 16:15 - 16:30     **I. Behrens, E. Peiner, K. Fricke, A. Bakin, A. Schlachetzki**  
Concept of a Byroscope in Hetero-Micromachining  
Techn. Univ. Braunschweig, Inst. für Halbleitertechnik, Germany
- 16:30 - 16:45     Break

### D2 Diamond Sensors

- 16:45 - 17:00     **P. Schmid, M. Adamschik, E. Kohn**  
Diamond Electromechanical Relais  
Univ. of Ulm, Dept. of Electron Devices and Circuits, Germany
- 17:00 - 17:15     **A. Perdochová**  
Diamond Radiation Detectors  
Slovak Univ. of Technology, Dept. of Nuclear Physics and Technology, Slovakia
- 17:15 - 17:30     **R. Zeisel, C.E. Nebel, M. Stutzmann**  
Characterisation of Radiation Damage in Type IIB Diamond by Capacitance Techniques  
Techn. Univ. München, WSI, Garching, Germany

# 10th European Heterostructure Technology Workshop

## Poster Session

17:30 - 19:00

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Post-Growth Annealing Effect on Magneto-Transport and Structural Properties  
of  $\text{Si}_{0.2}\text{Ge}/\text{Si}_{0.65}\text{Ge}_{0.35}/\text{Si}(001)$  Modulation Doped Heterostructure

**M. Kunze, E. Kohn**  
Growth and Characterization of Low Temperatures  
Univ. of Ulm, Dept. of Electron Devices & Circuits, Germany

**M. Neuburger, I. Daumiller, E. Kohn**  
Device Simulation and Characterization of GaN/InGaN/GaN Heterostructure FET  
Univ. of Ulm, Dept. of Electron Devices & Circuits, Germany

**R. Müller, M. Adamschik, A. Denisenko, E. Kohn**  
Diamond pH-Sensor  
Univ. of Ulm, Dept. of Electron Devices & Circuits, Germany

**Y. Guhel, B. Boudart, T. Heim, N. Grandjean\*, F. Omnes\*, J.C. De Jaeger**  
Dry etching for gate recessing on AlGaIn/GaN HEMT's

**J. Bendedikt, Paul J. Tasker**  
High Power Time Domain Measurement System with Active Harmonic  
Load-Pull for Base Station Amplifier Design  
Cardiff University, Cardiff, United Kingdom

**M. Lagadas\*, A. Müller\*\*, G. Konstantinidis\*, G. Deligeorgis\*, S. Iordanescu\*\*,  
I. Petrini\*\*, D. Vasilache\*\*, P. Blondy\*\*\***  
Low Temperature GaAs Micromachined Membranes as Support for MMIC  
passive Elements  
\* Forth IESL, Heraklion, \*\* IMT Bucharest, \*\*\*IRCOM Limoges

**S. Kiatgamilchai, M. Myronov, O.A. Mironov, E.H.C. Parker, T.E. Whall**  
A Novel Mobility Spectrum Maximum Entropy Approach for  
Magnetotransport Analysis of SiGe/Si Heterostructures  
Dept. of Physics, University of Warwick, Coventry, UK

# 10th European Heterostructure Technology Workshop

Tuesday, 19.09.00

## E1 Session E GaN HEMTs

8:00-8:30

**J. Würfl (invited)**  
**GaN High Power High Temperatures Devices**  
Ferdinand Braun Institut, Berlin, Germany

8:30-8:45

**V. Hoel, Y. Guhel, B. Boudart, C. Gaquière, J.C. De Jaeger**  
First Results of GaN MESFETs Realized on (111) Si  
IEMN, Lille, France

8:45-9:00

**I. Daumiller, E. Kohn, D. Theron\***  
Instabilities of GaN-based FETs  
Univ. of Ulm, Dept. of Electron Devices and Circuits  
\*IEMN, Lille, France

9:00-9:15

**F. Schaich, E. Chigaeva, W. Walthes, N. Wieser and M. Berroth**  
Bias dependent AlGaIn/GaN HEMT  
Univ. of Stuttgart, Inst. of Electr. & Optical Comm. Eng., Germany

9:15-9:30

**M. Marso, A. Fox, P. Kordos**  
Characterisation of AlGaIn/GaN 2DEG Structures by RoundHEMT Application  
ISI, Jülich, Germany

9:30-9:45

BREAK

## E2 GaN device technology

9:45-10:00

**B. Schineller, T. Schmitt, M. Deufel, J. Hofeld, G. Strauch, M. Heuken, H. Juergensen**  
Multiwafer 6 Inch MOVPE Planetary Reactor for Electronic Device Production  
AIXTRON AG, Aachen

10:00-10:15

**A. Chini, G. Meneghesso, E. Zanoni, M. Manfredi\*, M. Pavesi\*, B. Boudart\*\*, C. Gaquiere\*\***  
Deep Traps Related Effects in GaN MESFETs Grown on Sapphire Substrate  
\* University of Parma, Italy  
\*\* IEMN, Lille, France

10:15-10:30

**Y. Guhel, B. Boudart, T. Heim, N. Grandjean\*, F. Omnes\*, J.C. De Jaeger**  
Ohmic contacts studies on AlGaIn/GaN HEMT's  
IEMN, Lille, France  
\* CRHEA, Valbonne, France

10:30-10:45

**J. Skriniarova<sup>†</sup>, H.P. Bochm, H. Lüth, P. Kordos**  
Mesa etching and gate recessing of n-type GaN: Photoelectrochemical Approach  
ISI, Jülich, Germany  
<sup>†</sup> Slovak Univ. of Technology, Dept. of Microelectronics, Bratislava, Slovakia

10:45-11:15

BREAK

# 10th European Heterostructure Technology Workshop

Tuesday, 19.09.00

## Session F III V Devices

11:15-11:30

**T. Parenty<sup>1</sup>, S. Bollaert<sup>1</sup>, J. Mateos<sup>2</sup>, A. Cappy<sup>1</sup>**

Design and Realization of Sub-100nm Gate Length HEMTs

<sup>1</sup>IEMN, Lille, France

<sup>2</sup>Universidad de Salamanca, Dept. de Fisica Aplicada, Spain

11:30-11:45

**M. Boudrissa, Y. Cordier, D. Théron, J.C. De Jaeger**

Topology's Influence on Gate Ionisation Currents of a Quasi Enhancement-Mode

Al<sub>0,67</sub>In<sub>0,33</sub>As/ Ga<sub>0,66</sub>In<sub>0,34</sub>As metamorphic HEMT

IEMN, Lille, France

11:45-12:00

**R. Vandersmissen, K. van der Zanden\*, D. Schreurs, G. Borghs**

Hybrid Integration of Thinned Metamorphic HEMTs on Germanium

IMEC, ACSS/NM, Leuven, Belgium

\*Currently at Infineon Technologies, Munich

12:00-12:15

**A. Tönnemann, M. Marso, A. Förster, A. Fox, P. Kordos**

Pseudomorphic InGaAs/InAlAs/InP-HEMTs for Cryogenic Applications

Inst. f. Schicht- u. Ionentechnik (ISI), Jülich

12:15-12:30

**A. Guzman, J. Hernando, E. Luna, J.L. Sánchez-Rojas, J.M.G. Tijero, E. Calleja, E. Munoz**

**G. Vergara\*, M.T. Montojo\*, F.J. Sánchez\*, R. Almazán\*, M. Verdú\***

Optimization of AlGaAs/AlAs/GaAs Quantum Well Infrared Detector Structures

Dept. de Ingenieria Electrónica, ETSI, Madrid, Spain

\*Centro de Investigación y Desarrollo de la Armada, Madrid, Spain

12:30-12:45

**H. Thomas**

Heterobarrier Issues for AlInAs-GaInAs 1,5µm Lasers

Univ. of Wales, Electronics Division, Cardiff, UK

## **SESSION A**

**A1. III V Nitride Materials Growth**

**A2. Diamond Growth**

## Polarization Induced Effects in Group-III-Nitride Heterostructures and Devices

O. Ambacher, ambacher@wsi.tu-muenchen.de,

Walter Schottky Institute, TU-Munich, Am Coulombwall, 85748 Garching, Germany.

Two dimensional electron gases in GaN/Al<sub>x</sub>Ga<sub>1-x</sub>N/GaN heterostructures suitable for high electron mobility transistors (HEMT's) are induced by strong polarization induced effects. The sheet carrier concentration and the confinement of the two dimensional electron gases located close to one of the AlGa<sub>x</sub>N/GaN interfaces are sensitive to a high number of different physical properties such as polarity, alloy composition, strain, thickness and doping of the AlGa<sub>x</sub>N barrier. We have investigated the structural quality, the carrier concentration profiles and electrical transport properties of undoped and silicon doped transistor structures by a combination of high resolution X-ray diffraction, atomic force microscopy, PL-spectroscopy, Hall effect, C-V profiling and Shubnikov-de Haas measurements.

The investigated transistor structures with N- and Ga-face polarity were grown by metalorganic vapor phase (MOCVD) or plasma induced molecular beam epitaxy (PIMBE) covering a broad range of alloy compositions ( $0.15 < x < 0.6$ ) and barrier thicknesses between 100 and 500 Å. High electron mobilities of 1536 and 7520 cm<sup>2</sup>/Vs were observed for sheet carrier concentrations of  $1.1 \times 10^{13}$  cm<sup>-2</sup> at room temperature and 77 K, respectively.

We have calculated the polarization induced sheet charge based on different sets of piezoelectric constants available in the literature and the sheet carrier concentration self-consistently from a coupled Schrödinger and Poisson equation for different alloy compositions and degree of relaxation of the barrier. By comparison of theoretical and experimental results we demonstrate that the formation of two dimensional electron gases in undoped and doped AlGa<sub>x</sub>N/GaN structures both rely on the difference of piezoelectric and spontaneous polarization between the AlGa<sub>x</sub>N and the GaN layer. The maximum sheet carrier concentration for undoped HEMT's with a typical barrier thickness of 300 Å is limited to about  $2 \times 10^{13}$  cm<sup>-2</sup> due to strain relaxation and a reduction of piezoelectric polarization of the barrier. Even by heavy doping of the barrier ([Si] =  $10^{19}$  cm<sup>-3</sup>) the maximum sheet carrier concentration can only be increased by approximately 15%.

In addition, the measured dependence of electron mobility and saturation electron velocity versus sheet carrier concentration (covering the range between  $2 \times 10^{12}$  and  $2 \times 10^{13}$  cm<sup>-2</sup>) of doped and undoped HEMT's will be presented and the importance of interface roughness and charged dislocation scattering on electric transport will be discussed.

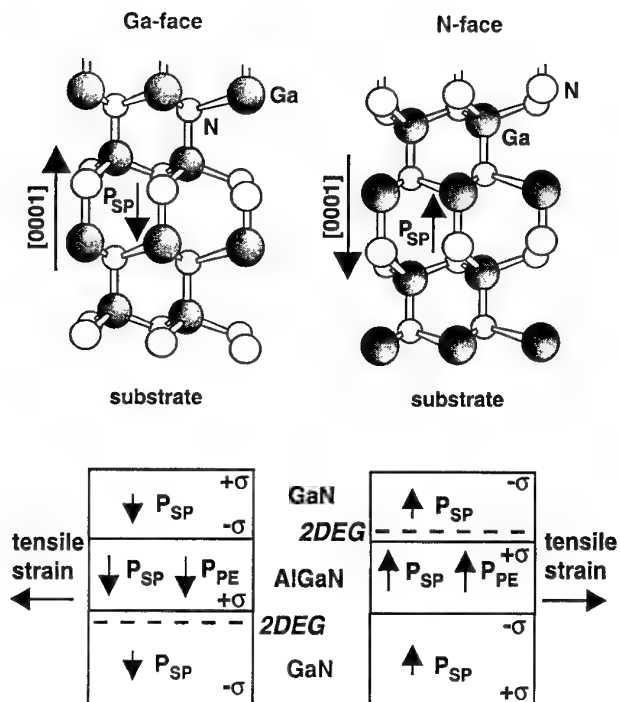


Fig.1: GaN with Ga-face and N-face polarity. The polarity determines the direction of spontaneous and piezoelectric polarization in GaN/AlGaIn/GaN HEMT structures and therefore the interface at which a 2DEG is confined.

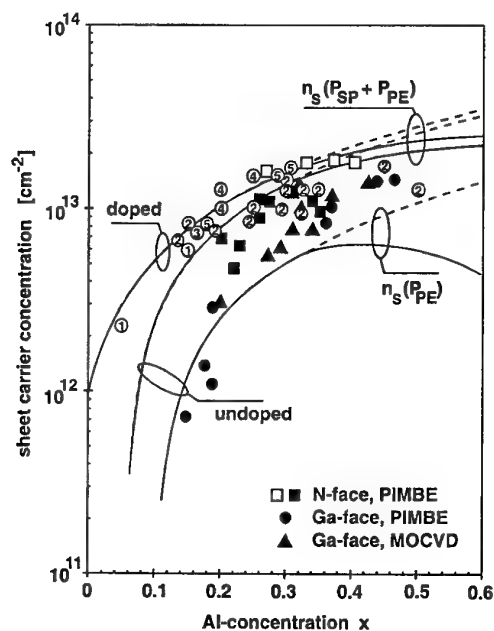


Fig.3: Calculated and measured sheet carrier concentrations for undoped (black symbols) and doped (white symbols) versus Al-concentration of the barrier.

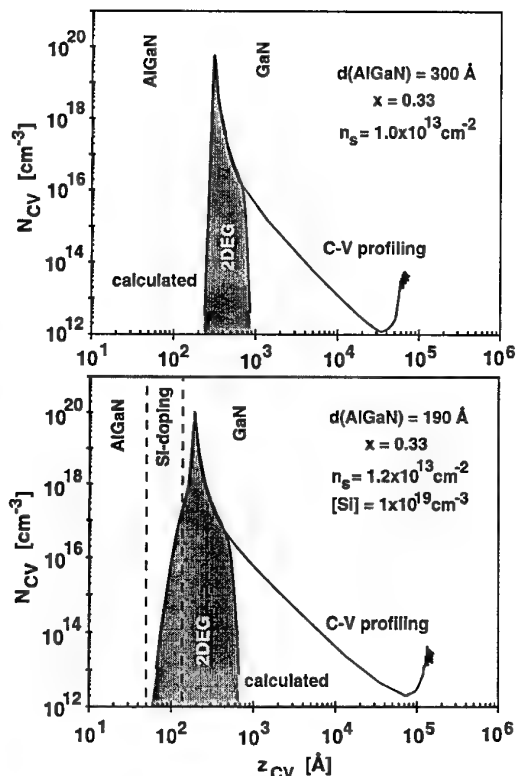


Fig.2: Calculated and measured carrier distribution of 2DEGs in pseudo-morphic, undoped and doped  $\text{Al}_{0.33}\text{Ga}_{0.67}\text{N}/\text{GaN}$  heterostructures with different barrier thickness.

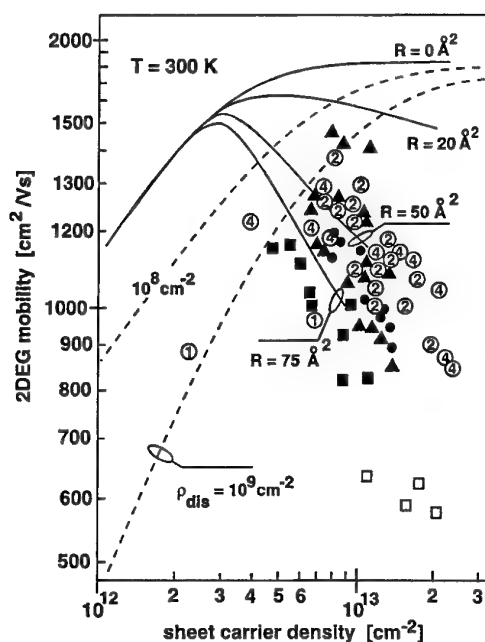


Fig.4: Calculated and measured room temperature Hall mobilities versus sheet carrier concentration. The 2DEG mobility is significantly affected by dislocation and interface roughness scattering.

## MOCVD Growth of III-V Nitrides for Electronic Applications: Problems and Special Features

M. Seyboth, C. Kirchner, M. Scherer, V. Schwegler, and M. Kamp  
University of Ulm, Department of Optoelectronics, 89069-Ulm, Germany

GaN-based materials, the alloys of GaN, InN and AlN, constitute today's fastest developing compound semiconductor technology. Their predicted market volume of approximately 3 billion USD will be about 20% of the total compound semiconductor turnover [1], with light-emitting diodes (LED) being the driving force behind this market.

The epitaxial building blocks developed for LEDs, however, cannot be simply transferred to electronic device structures. The different device geometries require lateral versus vertical current transport for example for field effect transistors (FETs) and LEDs, respectively. Furthermore, the buffer conductivity plays an important role for FETs in the high frequency range [2].

We elaborate specific requirements on metal organic chemical vapor deposition (MOCVD) for electronic applications related to the epitaxial growth of indium and aluminum containing layers.

Most optoelectronic devices do not require AlGaIn layers with Al-contents higher than 20% (i.e. a typical value for an electron barrier). For electronic devices Al-contents up to 100% [2] are desirable e.g. to extend the temperature range for device operation or increase the internal field in a piezo FET. For our growth system (Aixtron AIX 200RF) we found strong parasitic reactions limiting the growth of aluminum containing layers. We were able to develop a model based on prereactions between ammonia and the metalorganic precursors, which gives an explanation of the processes during growth, allows a precise growth control, and enabled high aluminum contents (Figure 1.).

The optimization of indium containing layers for optoelectronic devices is usually done on quantum film structures. These thin (<10nm) films are not suitable as channel structure for electronic devices. Thicker InGaIn layers tend to generate V-defects or even In-droplets. These kind of defects can act as scattering centers and thereby reduce the lateral mobility in the film. Higher growth temperatures can decrease these defect formation. Yet a simple temperature elevation reduces the In-content due to indium desorption and thus the carrier confinement is weakened. The influence of temperature and carrier gas (hydrogen vs. nitrogen) on indium content will be discussed (Figure 2.).

[1] Strategies Unlimited, *Visible LED Market Review and Forecast*, (1996).

[2] I. Daumiller, C. Kirchner, M. Kamp, K. J. Ebeling, E. Kohn, *Evaluation of Temperature Stability of AlGaIn/GaN Heterostructure FETs*, IEEE Electron Device Letters, Vol. 20, NO. 9 (1999).

[3] I. Daumiller, E. Kohn, C. Kirchner, M. Kamp, K.J. Ebeling, L. Pond, C.E. Wetzel, *DC and RF Characteristics of AlN/GaN Doped Channel Heterostructure Field Effect Transistors*, Electronics Letters, 35(18), 1588-1590 (1999).

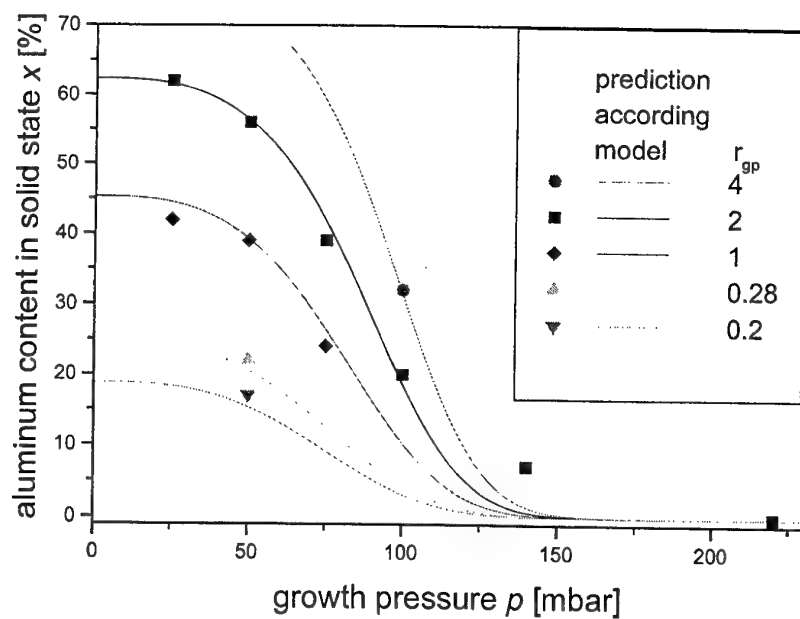


Figure 1. Aluminum content versus growth pressure: The comparison of model and experimental data reveals a good agreement in a large pressure range and variation of injected TMAI to TMGa ( $r_{gp}$ ).

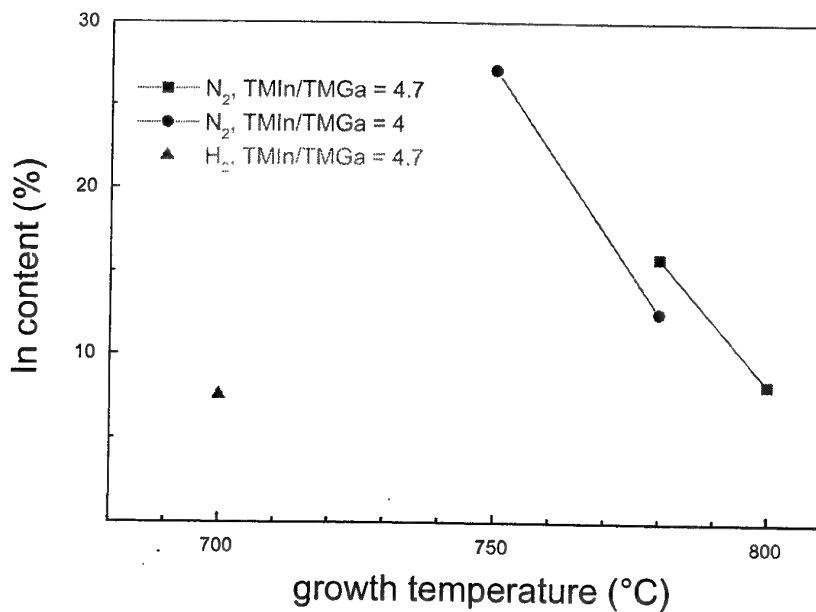


Figure 2. Indium content versus growth temperature for different carrier gases: Nitrogen compared to hydrogen allows for a temperature increase of about 100 K for the same indium content.

# Dry Etching Influence on Contact Formation to Gallium Nitride

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GaN and its ternary alloys with Al and In gained a large commercial interest as direct wide bandgap semiconductor materials. Their physical and chemical properties make them a promising material system for electronic devices like high power and/or high frequency FETs [1].

However, due to the physical and chemical inertness of GaN a wet-chemical etching process suitable for device fabrication is not available, although approaches like photo-enhanced wet-chemical etching proofed etching capabilities [2]. As device patterning is necessary for most applications dry etching techniques like reactive ion etching (RIE) or chemical assisted ion-beam etching (CAIBE) are almost solely used for device fabrication.

We report on the characterization of contacts to p- and n-type GaN with and without previous dry-etching of the semiconductor surface by CAIBE. For this experiments we use a CAIBE system with Ar as physical and Cl<sub>2</sub> as chemical etching component. To achieve sufficiently high etch rates, beyond 30 nm/min, a DC bias of 400 V is applied. For non-treated material, the contacts on the p- and the n-material had a specific contact resistance of  $\rho_{cp}=9 \times 10^{-3} \Omega \text{cm}^2$  and  $\rho_{cn}=1 \times 10^{-4} \Omega \text{cm}^2$  at a free carrier concentration of  $p=5 \times 10^{17} \text{cm}^{-3}$  and  $n=4 \times 10^{18} \text{cm}^{-3}$ , respectively.

IV-characteristics obtained on dry etched p-type GaN show a dramatic effect of the etching process on the contact behavior (Fig. 1). The change from ohmic to Schottky behavior of the contacts can be caused by CAIBE induced defects in the vicinity to the GaN surface. However, since AFM after etching reveals a defect related morphology, indicating that etching preferentially leaves disturbed (i.e. dislocation rich) material, this could also cause the Schottky behavior.

Contact alloying at 400 °C for 5 min does not significantly change the Schottky behavior. Similar results are obtained for n-type GaN, but here the current reduction is less severe.

[1] L. Eastman, presentation at EGW-4, Nottingham, 2000

[2] C. Youtsey et al., Appl. Phys. Lett. 72, pp.560, 1997

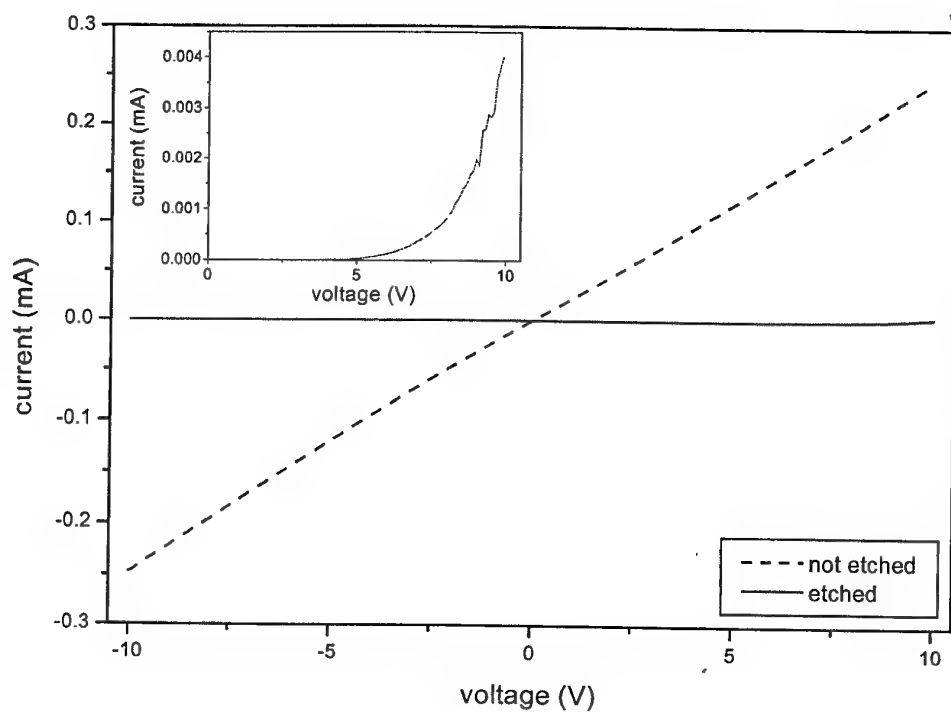


Figure 1: IV-characteristics of Ni/Au-contacts on etched and unetched Mg-doped GaN. Whereas on non-etched material the contacts show ohmic behavior, the contact behavior deteriorates dramatically on the etched material.

Growth dependent properties of GaN on Al<sub>2</sub>O<sub>3</sub> (0001) grown by radio frequency  
plasma-assisted molecular beam epitaxy

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Tsagaraki<sup>(1)</sup>, Z. Hatzopoulos<sup>(1)</sup>, and V. Yu. Davidov<sup>(2)</sup>

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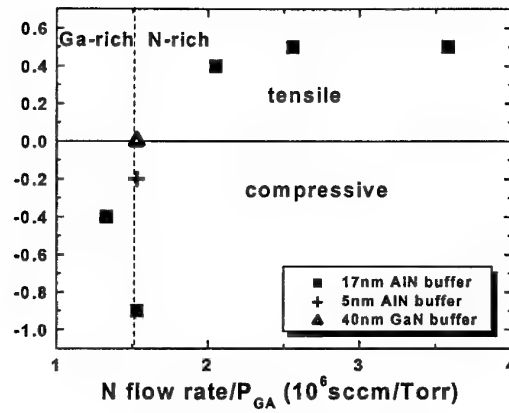
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One approach for the epitaxial growth of GaN is the method of Molecular Beam Epitaxy (MBE) using RF-plasma source for nitrogen activation (RFMBE). In this work, the structure, morphology, electrical and optical properties of heteroepitaxial GaN layers grown by RFMBE on c-plane sapphire, were investigated as a function of:

- (i) the V/III flux ratio and the type and thickness of the buffer layer (GaN or AlN), and
- (ii) the conditions for nitridation of the sapphire's surface.

First of all, the III/V flux ratio was found to have a significant effect on the surface morphology of the layers and a reduction of the rms surface roughness from 20nm to 3nm was achieved by decreasing the V/III ratio. However, the most remarkable observation, according to Raman scattering measurements, was the change of the sign of residual strain, in GaN layers with a 17nm AlN buffer layer, from tensile to compressive as the V/III ratio alters from N-rich to stoichiometric (or slightly Ga-rich) conditions (Fig. 1). The residual strain was significantly reduced for a thinner 5nm AlN buffer and it was zero for a 20nm GaN buffer. Stacking faults were observed only for significantly N-rich growth conditions.

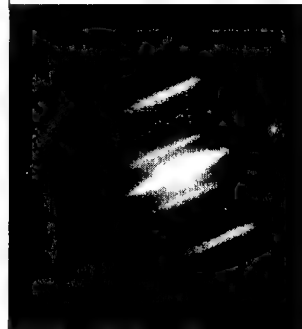
Two extremes and an intermediate condition of operating the rf-plasma source were compared for substrate nitridation at high or low substrate temperature. An important observation concerned the appearance of spotty RHEED patterns only during sapphire nitridation at high substrate temperature. In this case, the analysis of the evolution of the RHEED patterns during nitridation indicated a partially relaxed AlN on sapphire. However, even such a partial relaxation was not always observed for low temperature nitridation. The surface roughness of overgrown GaN layers depended basically on the III/V flux ratio and not of the nitridation treatment and streaky RHEED patterns could be obtained in both cases (Fig. 2). However, a significant observation concerned the potential control of the dominant polarity of the GaN layers by the substrate temperature during nitridation. RHEED observations (Fig. 2) suggested that high nitridation temperature apparently favours the Ga-face polarity (Fig. 2a), while low nitridation temperature favours the N-face (Fig. 2b). Electron microscopy observations however, revealed in both cases, the presence of inversion domain boundaries.



**Figure 1.** The in-plane biaxial residual stress of the GaN-on- $Al_2O_3$  (0001) epilayers has been plotted versus the N/Ga flux ratio. Different symbols have been used to distinguish the different types of used buffer layers.



(a)



(b)

**Figure 2.** RHEED patterns observed at the end of GaN-on- $Al_2O_3$  MBE growth: (a) x2 reconstruction for GaN grown with high temperature nitridation and (b) x3 reconstruction for GaN grown with low temperature nitridation.

## AlGaIn/GaN FETs: Performance and Problems

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The DC, small signal and power performance of AlGaIn/GaN HFETs grown on sapphire and s.i. SiC substrates will be presented. Investigation of the device results reveals that apart of the thermal properties related to the substrate material, also processing, measurement conditions and "biasing history" strongly influences the achieved performance.

Although the DC and small signal characteristics of the FETs on different substrates are very similar, it was found that the sapphire based devices are strongly limited in their performance at a high level of power dissipation, either under large signal RF operation or high DC-bias. However, it was observed that even devices on SiC encounter thermal limitations and that the output power density is sensitive to the device layout (figure 1) and therefore to the thermal impedance. Due to the excellent quality of the s.i. SiC epilayers, a record transconductance of 300mS/mm for 0.3 $\mu$ m gate-length, an  $f_t$  of 40GHz and an  $f_{max}$  of 80GHz were measured. Also the best power results were achieved on SiC-substrates (figure 2). At 10GHz a maximum output power of 36.5dBm (2.8W/mm) was measured with an unpassivated 1.6mm FET. At 20GHz small devices (2x100 $\mu$ m) yield approx. 3.3W/mm. The results indicate that the maximum output power is seriously limited by the current slump effect, as only about 50% of the power density expected from DC characterization is achieved. First experiments using a SiN passivation reveal slightly degraded performance with respect to gate leakage current and small signal performance. However, enhanced output power, breakdown voltage and drain current for passivated devices grown on sapphire substrates was achieved (figure 3 and 4). For FETs with gatelength of 1.2 $\mu$ m the increase in output power is more than 100% compared to unpassivated devices.

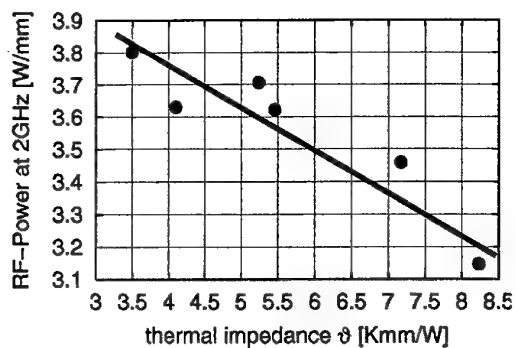


Figure 1 demonstrates the dependence of rf-power against thermal impedance on a SiC substrate. The thermal impedance depends strongly on the layout of the devices

Figure 2 shows the best power measurement at 10 GHz

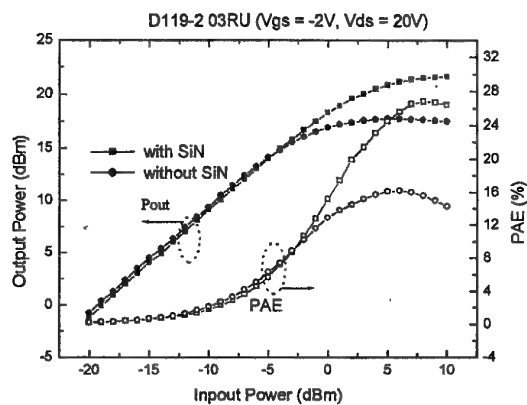
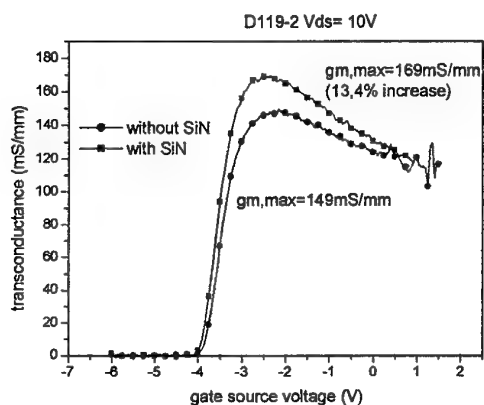
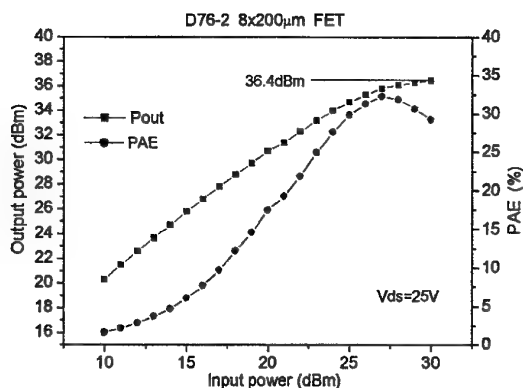


Figure 3 and 4 shows the influence of SiN passivation on the DC and power performance of a 2x50μm device. The gatelength is 1.2μm.

# Growth of Oriented Diamond Thin Films on Si (100) with Semiconductor Quality

K. Janischowsky, M. Stammer, F. Maier, and L. Ley

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Highly oriented diamond films on Si (001) substrates are available on wafers up to 2" diameter and well suited for micromechanical devices. However, integrating electronic devices on CVD diamond requires a crystalline structure of the film that does not impair its operation by grain boundaries or other imperfections, as they are usually present in nearly all of the oriented diamond films grown in microwave CVD systems.

To improve the structural quality of the diamond films we developed a hybrid process. The first stage of the diamond growth process was performed in a tubular MW-CVD system and involved a cleaning of the Si (001) sample with a hydrogen plasma, a bias pretreatment to achieve oriented nucleation over the whole substrate area (1 cm<sup>2</sup>) and finally a growth of several hours. After SEM investigation (Fig. 1a), the samples were transferred to a hot filament CVD system and the deposition continued for several tens of hours under conditions with no nitrogen addition and low methane concentration in the gas phase.

The sequential growth process yields closely packed crystallites with (001) surfaces that show no grain boundaries over areas of up to 60000  $\mu\text{m}^2$  by scanning electron microscopy (Fig. 1b). The diamond crystallites have the same orientation as the Si (001) substrate and their orientational order and surface quality as measured by low energy electron diffraction is comparable to that of single crystal diamond. Micro-Raman spectroscopy exhibits an exceptional quality of the film surface by the complete absence of a luminescence background and nitrogen vacancy complexes, as well as the absence of spectral features attributed to non-diamond carbon phases (Fig. 2). The electronic structure of the diamond film was investigated by angle resolved photoemission, which probes the valence band structure at the surface to a depth of 2 nm (Fig. 3). The main difference between the single crystal spectrum (left) and an oriented diamond film after the hybrid process (center) is a small shift towards higher binding energies due to residual film charging. Nevertheless, the valence band states of the film exhibit a clear dispersion, nearly indistinguishable from the single crystal (001) surface. Especially a non-dispersing background contribution from disordered parts as in the right spectrum is completely absent, which confirms the superior electronic quality of the CVD diamond film.

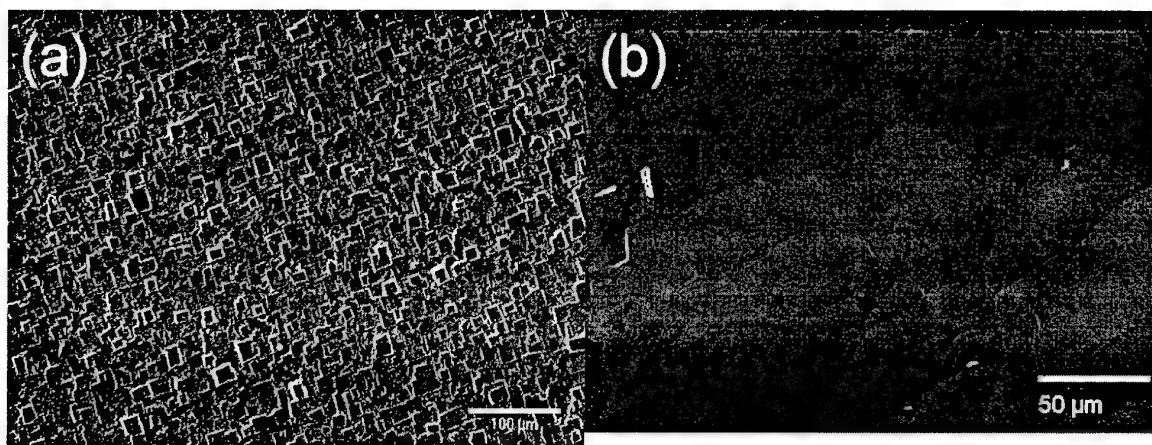


Fig.1: SEM micrograph of an oriented textured diamond CVD film on Si (100) grown in a MW system (a). The surface consists of a close tiling of square {100} surfaces separated by intermediate {111} facets. After the combined growth process in the HFCVD system, the micrograph shows a {100} surface with only a few {111} facets interspersed (b).

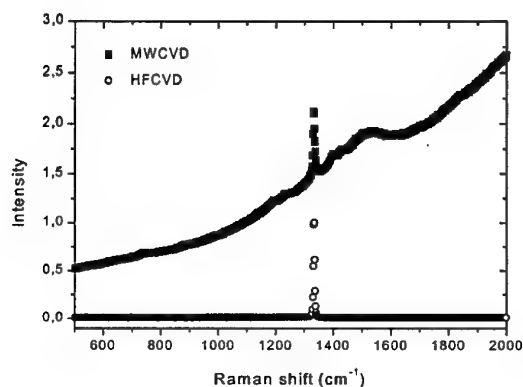


Fig. 2: Comparison of normalized Micro-Raman spectra from a MW deposited diamond film with a HF overgrown film. Whereas the spectrum of the HF grown film is comparable to single crystalline diamond, the MW grown film exhibits contributions of amorphous carbon (around  $1500\text{ cm}^{-1}$ ) and a strong luminescence background due to a variety of defects.

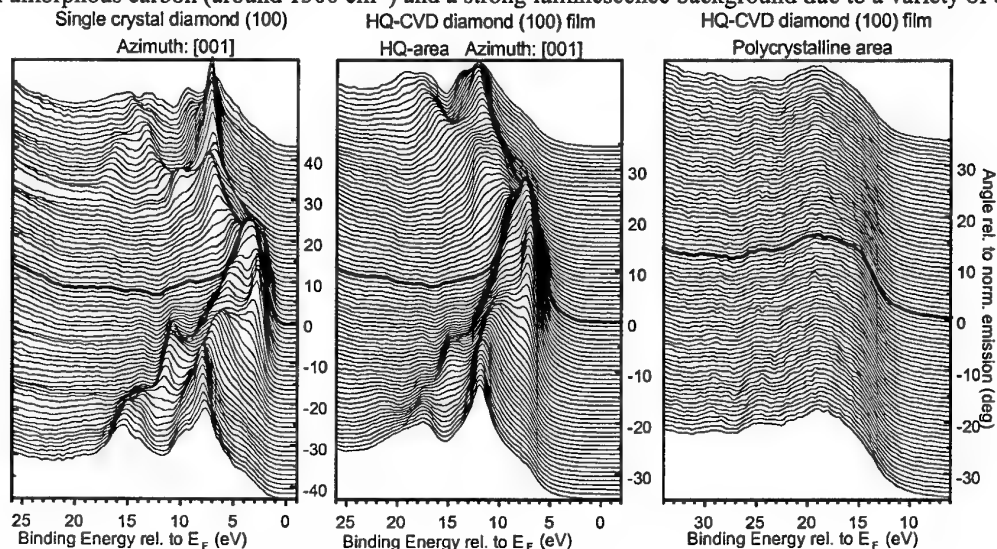


Fig. 3: Electronic structure of the diamond valence band for different surfaces. In a polycrystalline film (right spectrum) only the density of states is detectable. In contrast, the spectrum of an {100} oriented film (center) after the sequential growth process is - beside a slight charging - nearly indistinguishable from the spectrum of a natural single crystal diamond (left).

# Electron Assisted Hot-Filament CVD Deposition of Diamond Films

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## Abstract

In this study, a new deposition apparatus is presented to grow diamond thin films. The used hybrid hot-filament chemical vapor deposition (HF CVD) technique extends the standard one in ability *i)* to produce positively charged ions, *ii)* to easy separate and control growth steps (nucleation and growth), and *iii)* to adjust dosage of ion bombardment onto the substrate. The reactor allows igniting of dc plasma between the hot filaments and a conductive grid placed above the filaments (in forward biasing), as shown in Fig.1. In addition, d.c. source placed between the filaments and substrate allows to control a substrate bombardment by either positive ions (in reverse biasing) or electrons (in forward biasing). Such an arrangement results in stable process conditions and reproducible deposition. Furthermore, the influence of electron bombardment during the growth stage on possible lowering of activation energy of diamond growth is discussed. Diamond thin films were grown on mirror polished silicon wafers. During the nucleation step, all process parameters (gas pressure, substrate biasing, nucleation time, etc.) were kept constant for all samples to enhance better understanding of the growth process. So, the influence of substrate temperature on the diamond growth has been studied independently of nucleation effects. The activation energy ( $E_a$ ) of the growth process was calculated from the slope of the Arrhenius plot of the growth rate vs. reciprocal temperature. The activation energy is  $E_a = 2.5$  kcal/mol for the temperature range of 600 – 900 °C at positive substrate bias of +100 V (Fig.2). This value of the activation energy is smaller than 5.85 kcal/mol and 8.6 kcal/mol previously reported in [1] and [2], respectively. Yamaguchi et al. reported activation energy as small as 1 – 5 kcal/mol only for low substrate temperatures ranging from 210 to 700 °C [3]. However, this activation energy increases up to 12.5 kcal/mol in the case of grounded substrate, as shown in Fig. 2. The lowering of the activation energy down to 2.5 kcal/mol at substrate temperatures above 600 °C is attributed to electron-assisted diamond growth. Furthermore, this result indicates possible change in growth mechanism and the two-step  $C_2$  addition mechanism [1] seems to be a dominant process in contrast to generally accepted models based on hydrogen abstraction and  $CH_3$  growth specie [4].

**Keywords :** diamond growth, chemical vapor deposition, activation energy

## References

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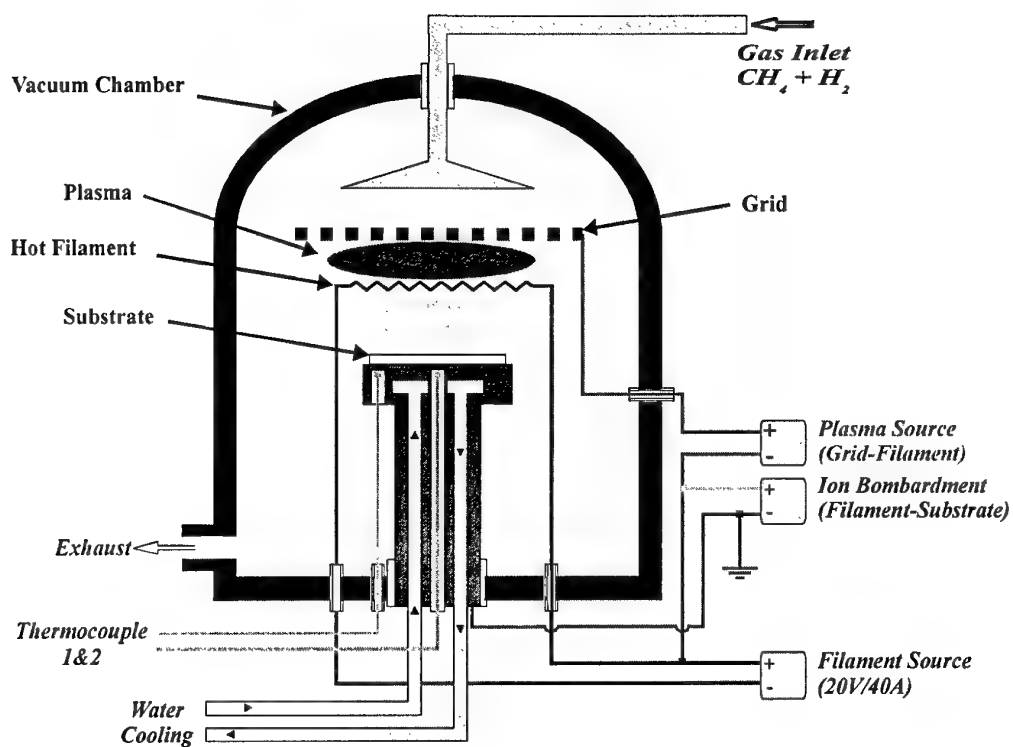


Fig. 1: A block view of hybrid hot-filament apparatus

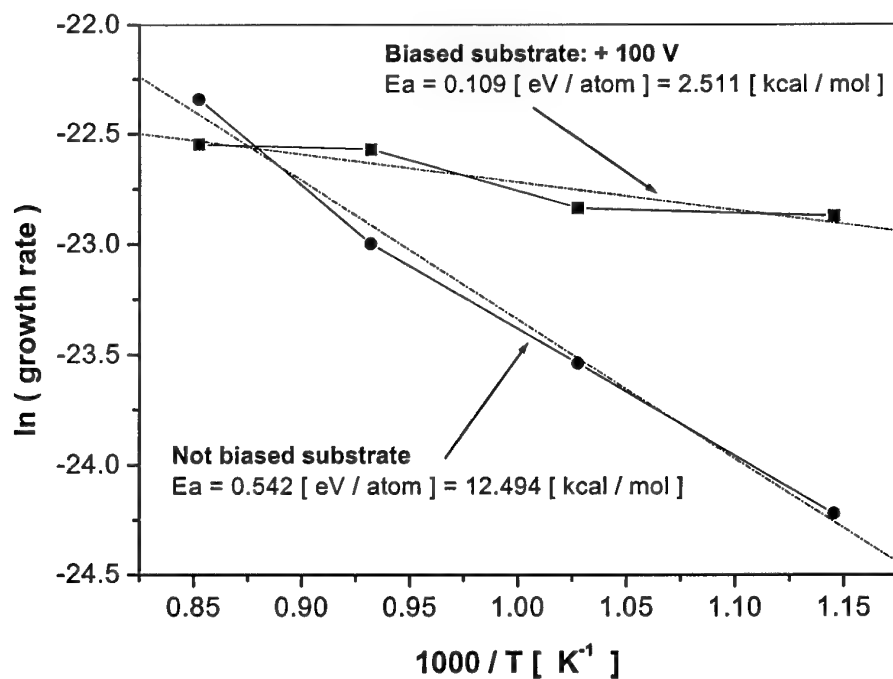


Fig. 2: Arrhenius plot of the natural logarithm of the linear growth rate vs. reciprocal substrate temperature for diamond films deposition at i) positively biased and ii) grounded substrate.

# TEMPERATURE DEPENDENCE OF QUALITY FOR DIAMOND THIN FILMS DEPOSITED ON Si (100) VIA DOUBLE BIAS-ASSISTED HFCVD

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## ABSTRACT

In recent years, the deposition techniques for diamond films have progressed rapidly. However, one of major problems with silicon and other substrates is low nucleation density in the absence of nucleation pretreatment. Thus, mirror-finished silicon substrates are usually scratched with diamond powder prior to chemical vapor deposition. This procedure is not suitable for optical applications and there is an interest to find another methods leading to high nucleation density of diamond on Si substrates.

Yugo et al. [1] firstly suggested bias-enhanced diamond nucleation in a microwave plasma CVD. Recently, X. T. Zhou et al. [2] have reported the use of two bias voltage in the hot filament chemical vapor deposition (HFCVD) apparatus to obtain high reproducible heteroepitaxial diamond nucleation on Si(100). Using this method a high nucleation density of textured diamond on mirror-polished Si (100) substrate can be achieved.

We have investigated the effect of substrate temperature in the range 600 and 900 °C on the quality of diamond thin films prepared by double bias-assisted hot filament chemical vapor deposition (HFCVD) method [3]. A double bias-assisted HFCVD represents an advanced technology in the preparation of diamond films. Ions in the plasma are driven to substrate by a negative substrate bias voltage. In the process, a negative bias voltage is applied to the Si wafer and positive bias voltage is applied to a grid placed on top of the hot filaments. A substrate is placed on a rotating substrate holder to support a homogeneity of deposited films. We first report the influence of the substrate temperature on the quality of deposited Si wafers in such a double bias-assisted HFCVD system. The films were characterized using micro-Raman spectroscopy. Micro-Raman spectra (Fig.1.) showed a very sharp peak centered near the natural diamond line ( $\sim 1332 \text{ cm}^{-1}$ ) at low temperature range (600-700 °C).

**Keywords :** Micro-Raman spectra; Bias-assisted hot filament chemical vapor deposition; Diamond

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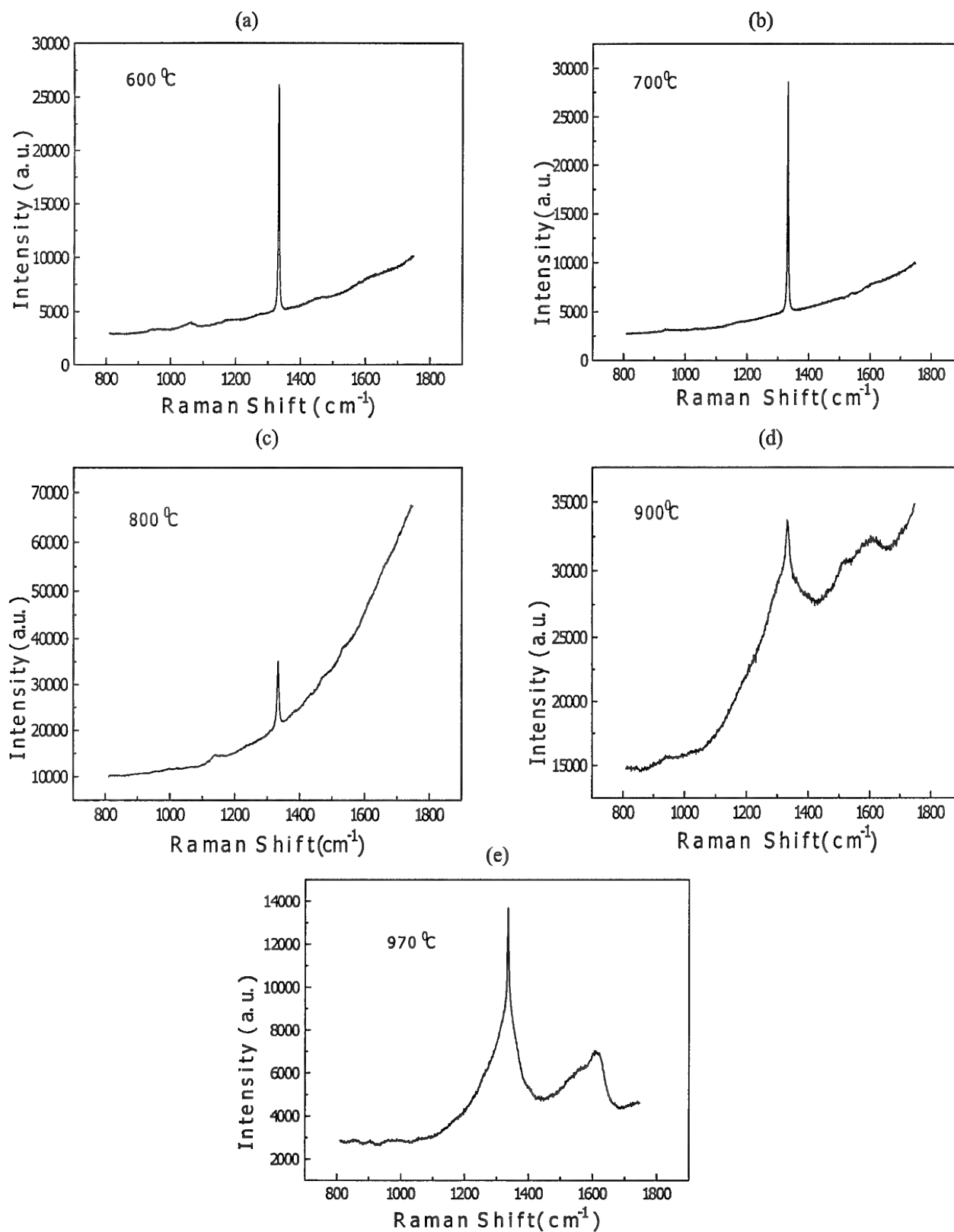


Fig.1. Typical Raman spectra of diamond films deposited at (a) 600 degrees Celsius. (b) 700 degrees Celsius. (c) 800 degrees Celsius. (d) 900 degrees Celsius. (e) 970 degrees Celsius.

## **SESSION B**

### **SiGe Devices**

# Investigation of hot carrier induced degradations in microwave SiGe HBTs

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## 1. Introduction

The emergence of SiGe heterojunction transistor as a contender for the next wireless applications is now well established. In order to meet with the frequencies allocated which range from 1 GHz to 80 GHz, it is necessary to develop SiGe technologies featuring frequency performances larger than 100 GHz. The heterojunction concept dealt to speed up the conventional bipolar technologies. To go to higher frequency, it is necessary to shrink the devices which could turn to some spurious behaviour.

The purpose of this paper is to assess some reliability behaviour associated with the new shrunk SiGe HBT devices. One critical point related to the small dimensions deals with the behaviour of the emitter base (EB) junction reverse bias stressed and its impact on the electrical properties of the device in term of frequency performances, DC and low frequency noise behaviour. In order to get a better understanding, the experimental data will be supported by physical simulations.

## 2. Results and discussion

Reverse bias stress experiments at the emitter base junction have been carried out with stress charge ranging up to 3.5 V. The experiments have been performed on a set of five SiGe BiCMOS HBT featuring  $0.8 \mu\text{m} \times 25 \mu\text{m}$  emitter size. The stress impact has been evaluated by DC, S parameters and low frequency noise measurements.

Fig. 1 shows the base current evolution versus stress from the forward Gummel plot measurements. We can observe the decrease of the current gain associated to a rise up of the base current, more precisely the shape of the base current after the stress is showing a non ideal component (featuring an ideality factor of 2). At lower current level, the base current component exhibits an ideality factor of 3.3. We have to note that the collector current remains a constant value with respect to the stress. This behaviour suggests that the reverse emitter base stress creates some defects and traps located at the emitter base region (in the spacer oxide along the emitter perimeter). In order to validate this assumption, we made some physical simulation using the Blaze device simulation software by Silvaco.

Fig. 2 represents a cross section of the simulated device. The doping level and profile of emitter, base and collector region are reported in fig. 3. The Ge content of the base layer is 12 % in the collector-near region and graded from 12 % to 0 % in the emitter-near region. The non ideal base current component featuring an ideality factor of 2 has been assessed by introducing surface recombination close to the emitter perimeter as plotted in figure 2. On the other hand, the base current component in the very low bias range has been attributed to tunneling current assisted by band-gap traps created during the stress.

Fig 1 compares experiments and simulation where we can observe a good agreement which validates our assumptions. We report that the stress leads to a surface recombination rate increasing from  $2.0 \cdot 10^6 \text{ cm/s}$  to  $3.0 \cdot 10^6 \text{ cm/s}$ , and a pre-exponential factor of the tunneling current ranging from 0 to  $6.0 \cdot 10^{-10}$ .

Fig. 4 shows the effect of the stress on the  $S_{21}$  parameter measured before and after the stress procedure. A decrease of the magnitude of  $S_{21}$  is reported if the base current is kept at a constant value (when measurements are carried out at the same collector current no variation is observed). The other S parameters were nearly not affected by the applied stress regardless if the base current or the collector current is kept constant. More explanation will be given at the conference. Again, the S parameters degradation was addressed by means of physical simulations. The numerical simulations confirmed that the main effect of the stress is a reduction in magnitude of  $S_{21}$  while the other parameters remain unaffected. In particular, it is worth pointing out that also the simulations show that the changes in  $S_{21}$  are minimised if the collector current is kept constant before and after the stress.

The last parameter we focussed on deals with the low frequency noise behaviour which has been assessed by the measurement of the input noise current generator (which represents the base current fluctuation). Fig. 5 shows the frequency evolution (100 Hz-100 kHz) of the input current noise generator versus stress experiments. We can observe that the stress turns to a strong degradation of the  $1/f$  noise component which is relevant with traps and recombination created along the emitter perimeter. The  $1/f$  noise factor-of-merit  $B_{1/f}$  rises from  $8.26 \cdot 10^{-21} \text{ m}^2$  to  $4.19 \cdot 10^{-19} \text{ m}^2$  (both are average values in the range up to  $10^4 \text{ Hz}$ ).

## 3. Conclusion

In the present work the degradations induced by applying reverse base-emitter bias stresses to SiGe HBTs were investigated by both simulations and DC, RF, and LFN measurements. The results of simulation and measurements were compared and good agreement was observed. The simulations of the DC effects pointed out that the degradations are due to the increase of surface recombination close to the emitter perimeter and to the rise up of tunneling assisted by mid-gap traps. As for the microwave characteristics, both simulations and experiments revealed that the main effect is the decrease of the magnitude of  $S_{21}$  and that this degradation is minimised if the base current is kept constant.

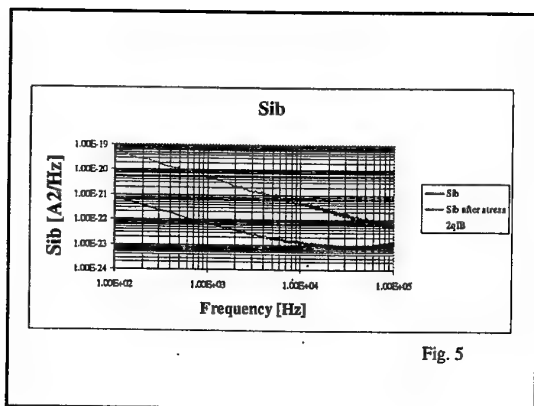
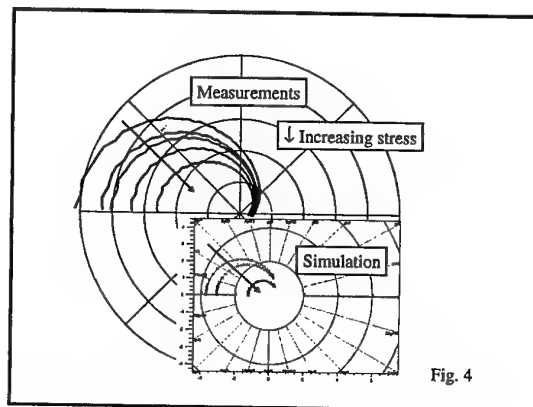
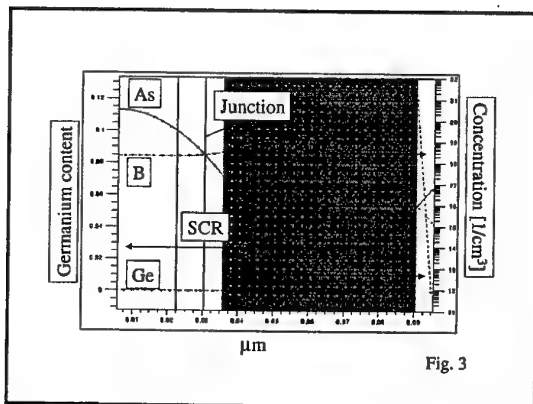
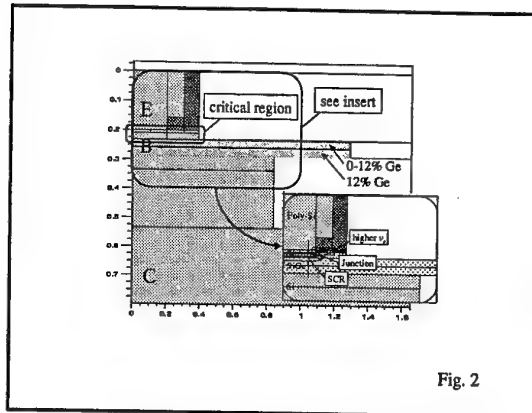
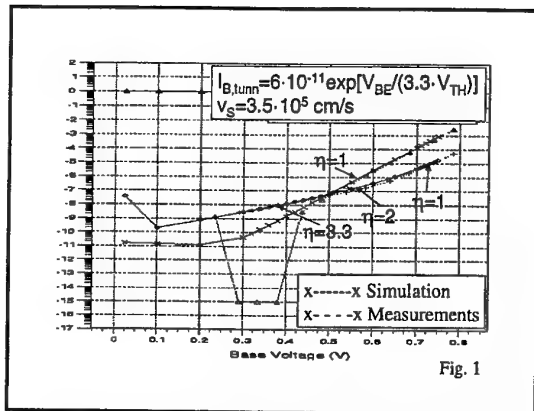
The LFN measurements well pointed out the HBT degradation. The merge with the simulations allowed to quantitatively associate the large increase of the  $1/f$  noise factor-of-merit with the increase of the surface recombination rate and with the presence of tunneling assisted base current components.

## 4. Acknowledgements

This work is supported by TMR network entitled "Advanced SiGe heterodevices".

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# Thermal annealing effect on properties of $\text{Si}_{0.2}\text{Ge}_{0.8}/\text{Si}_{0.7}\text{Ge}_{0.3}/\text{Si}(001)$ p-type modulation doped heterostructures

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When growing high Ge content  $\text{Si}_{1-x}\text{Ge}_x$  channels by SS-MBE it is advantageous to use low growth temperatures to kinetically suppress surface segregation, which smears the Ge profile, and also to suppress surface diffusion that can produce roughness of the surface to relieve strain energy. This study concerns the recovery by post-growth furnace thermal annealing at temperatures 600-900°C for 30min of magneto-transport properties of heterostructures with  $\text{Si}_{0.2}\text{Ge}_{0.8}$  channels grown at 300°C. The effect of thermal annealing on the properties of  $\text{Si}_{0.2}\text{Ge}_{0.8}/\text{Si}_{0.7}\text{Ge}_{0.3}/\text{Si}(001)$  p-type modulation doped heterostructures with 10nm (sample "A") and 14nm (sample "B")  $\text{Si}_{0.2}\text{Ge}_{0.8}$  channel thicknesses was studied by magneto-transport measurements, XTEM and Raman spectroscopy. The heterostructures were grown on Si(001) substrates by SS-MBE in a VG Semicon V90S system. The  $\text{Si}_{0.2}\text{Ge}_{0.8}$  channel was grown on an 850nm thick virtual substrate involving a low-temperature Si buffer [1], which was relaxed to the lattice constant of  $\text{Si}_{0.7}\text{Ge}_{0.3}$ .

The mobility and sheet carrier density of as-grown and annealed samples were obtained by a combination of resistivity and Hall effect measurements in the temperature range of 9-300K. Annealing at 600°C is seen to have a negligible effect on the mobility. Increasing the annealing temperature results in pronounced successive increases of mobility. For both the heterostructures the highest mobilities at 9K and at 300K were observed after annealing at 750°C. The best mobility was obtained in sample "A". At 9K we observed an increase of mobility (at sheet carrier density) from  $625\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$  ( $1.37\cdot 10^{12}\text{cm}^{-2}$ ) in the as-grown sample up to  $1680\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$  ( $1.57\cdot 10^{12}\text{cm}^{-2}$ ) in the annealed one, and at 300K from  $170\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$  ( $2.6\cdot 10^{12}\text{cm}^{-2}$ ) up to  $512\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$  ( $2.11\cdot 10^{12}\text{cm}^{-2}$ ).

Cross-sectional TEM was performed on the as-grown and annealed heterostructures to determine the structural integrity of the epilayers and the dislocation microstructure in relaxed virtual substrates. In the annealed samples we observed broadening of the  $\text{Si}_{0.2}\text{Ge}_{0.8}$  channel, accompanied by a reduction of the Ge content.

The very same as-grown and annealed samples studied by magneto-transport were characterized by Raman spectroscopy at 293K. In Raman spectra of as-grown samples in addition to Ge-Ge, Si-Ge and Si-Si phonon modes originated from  $\text{Si}_{0.7}\text{Ge}_{0.3}$  epilayers, we clearly observed the Ge-Ge mode from  $\text{Si}_{0.2}\text{Ge}_{0.8}$  layer (channel). After annealing, significant changes in position as well as intensity were observed for the Ge-Ge mode originating from the channel, which allows us to estimate a degree of relaxation in the channel and upper epilayers of the virtual substrate. This demonstrates the sensitivity of the Raman spectra to interdiffusion during annealing in the buffer/channel/spacer region.

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## Low frequency noise in Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si heterostructure p-channel MOSFETs

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### Abstract

Low frequency drain current noise is investigated in Si/Si<sub>0.64</sub>Ge<sub>0.36</sub>/Si and Si control p-MOSFETs. Growth and processing details are given elsewhere<sup>1</sup>. Measurements are performed in the linear region of MOSFET operation. Noise power spectral densities,  $S_I(f)$  have been fitted to a flicker noise ( $1/f^\gamma$ ) component plus a sum of Lorentzian generation-recombination (g-r) components and a thermal noise component (figure 1). Flicker noise dominates at low frequencies and is more than a decade lower for devices with a SiGe channel (figures 2 & 3). Flicker noise amplitude scales inversely with channel length, as shown in figure 3. The lower flicker noise in SiGe channel devices is thought to be due to the separation of charge carriers from traps at the oxide interface<sup>2</sup>. The exponent of the flicker noise  $\gamma$  varies between 0.84 and 1.25 and tends to increase with flicker noise amplitude. The thermal noise of all the devices measured was found to be inversely proportional to their channel resistance, with a slope of  $1.28 \cdot 4kT$ , as shown in figure 4. Channel resistances were taken from the slope of drain current-voltage plots. Measurements of noise versus gate voltage show peaks which are believed to correspond to trap levels at the oxide interface<sup>3</sup> (figure 5). It has been proposed that flicker noise amplitude should vary with cap thickness for MOSFETs with SiGe channels<sup>2</sup>, however, no such dependence has been found (figure 6). Noise results are discussed in terms of valence band offset and charge tunneling to trap states within the oxide.

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<sup>1</sup> G. Braithwaite et al. To be published.

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<sup>3</sup> Fu H., Sah, C. IEEE ED 19 pp. 273-284

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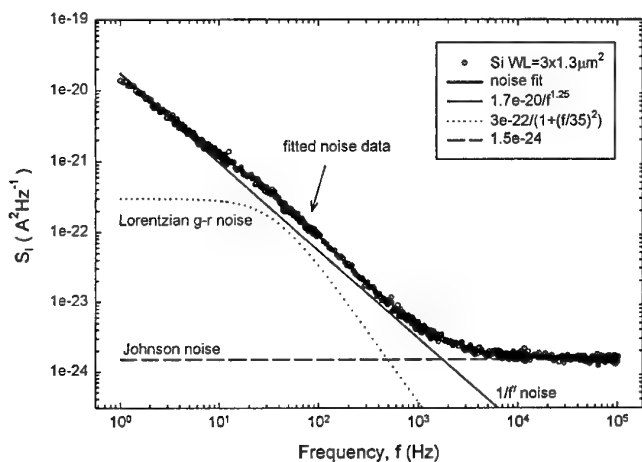


Figure 1: Example fit, Si FET WL=3x1.3μm<sup>2</sup> with one Lorentzian,  $A/(1+(f/f_0)^2)$

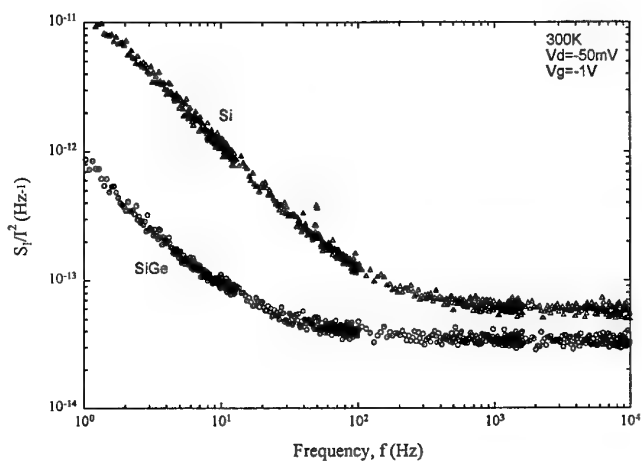


Figure 2: WL=40x10μm<sup>2</sup> Si & SiGe noise power spectral density

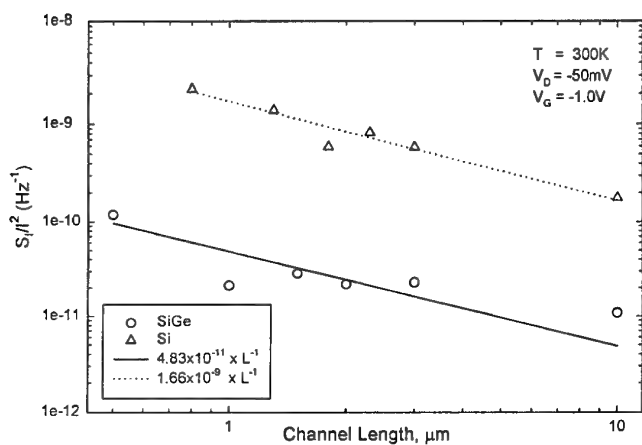


Figure 3: Si & Si<sub>0.64</sub>Ge<sub>0.36</sub> p-MOSFETs, 3μm wide,  $1/f$  component noise at 1 Hz

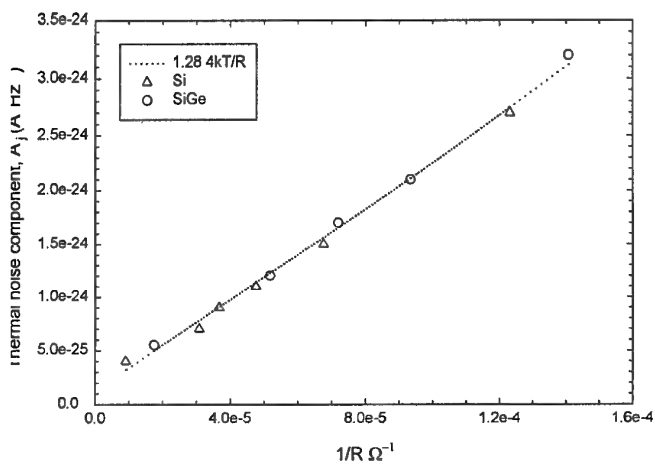


Figure 4: Thermal noise component of devices against channel conductance.

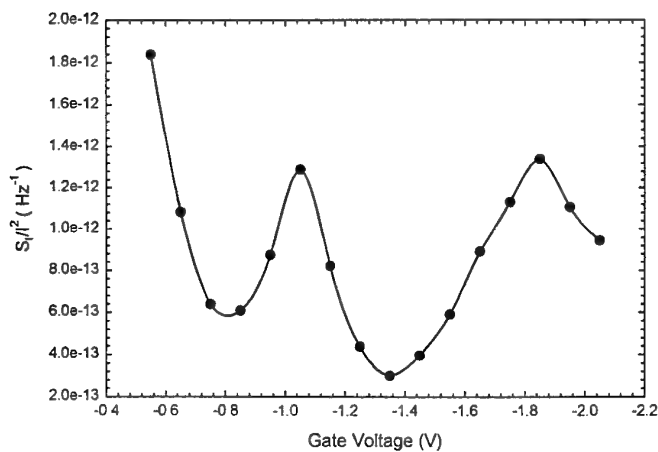


Figure 5: Si/Si<sub>0.64</sub>Ge<sub>0.36</sub> 5nm cap  $S_i$  @ 80Hz WL=3x0.8μm<sup>2</sup>

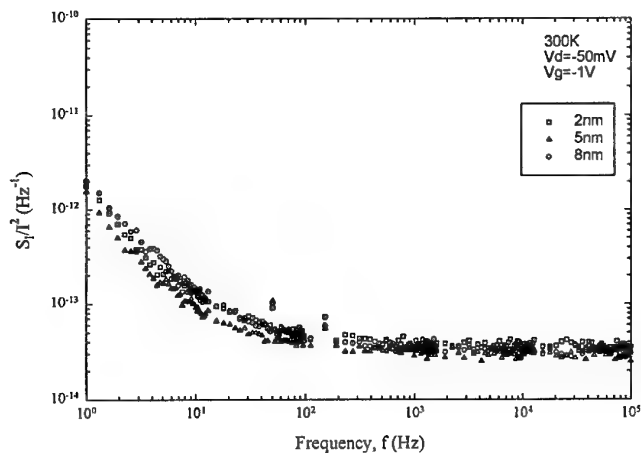


Figure 6: SiGe WL=40x10μm<sup>2</sup> noise in samples of varying cap thickness

# Magneto-transport properties of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}_{1-y}\text{Ge}_y/\text{Si}(001)$ p-type modulation doped heterostructures with high Ge content channel

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The magneto-transport properties of  $\text{Si}_{0.05}\text{Ge}_{0.95}/\text{Si}_{0.37}\text{Ge}_{0.63}/\text{Si}(001)$  (Sample A) and  $\text{Si}_{0.18}\text{Ge}_{0.82}/\text{Si}_{0.47}\text{Ge}_{0.53}/\text{Si}(001)$  (Sample B) modulation boron-doped heterostructures grown by solid source MBE are reported. Hall-bars with length to width ratio  $535\mu\text{m}/54\mu\text{m}$  were fabricated by dry etching in  $\text{SF}_6/\text{O}_2$  plasma and ohmic contacts were formed by evaporation of Pt/Au (20nm/200nm) followed by alloying at  $290^\circ\text{C}$  in  $\text{N}_2$  ambient for 30s.

The Hall mobility and sheet carrier density of the samples were obtained by a combination of resistivity and Hall effect measurements in the temperature range of 0.348-300K. The measured at 9K hole mobilities (at sheet carrier density) are  $9300 \text{ cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$  ( $1.58\cdot 10^{12} \text{ cm}^{-2}$ ) and  $5590 \text{ cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$  ( $1.13\cdot 10^{12} \text{ cm}^{-2}$ ) for samples A and B respectively. At temperatures 30-300K with the help of newly developed mobility spectrum analysis technique [1] carrier density and mobility of (i) two-dimensional hole gas (2DHG) carriers, (ii) boron-supply carriers, and (iii) electron-like carriers are obtained. The technique utilises the magnetic-field dependence of resistivity tensor and give us spectra, which encode the information about holes constant-energy surface in the strained SiGe channel. Below 20K in both samples we observed Shubnikov de Haas oscillations (SdH) (Fig. 1 and 2) that corresponds to the high quality of the grown structures. From this data the effective mass and the ratio of quantum to transport life times of 2DHG formed in the  $\text{Si}_{0.05}\text{Ge}_{0.95}$  and  $\text{Si}_{0.18}\text{Ge}_{0.82}$  channels close to top interface were extracted by method similar to [2]. The sheet carrier density of 2DHG extracted from SdH oscillations and low magnetic field Hall resistance for each sample is in good agreement.

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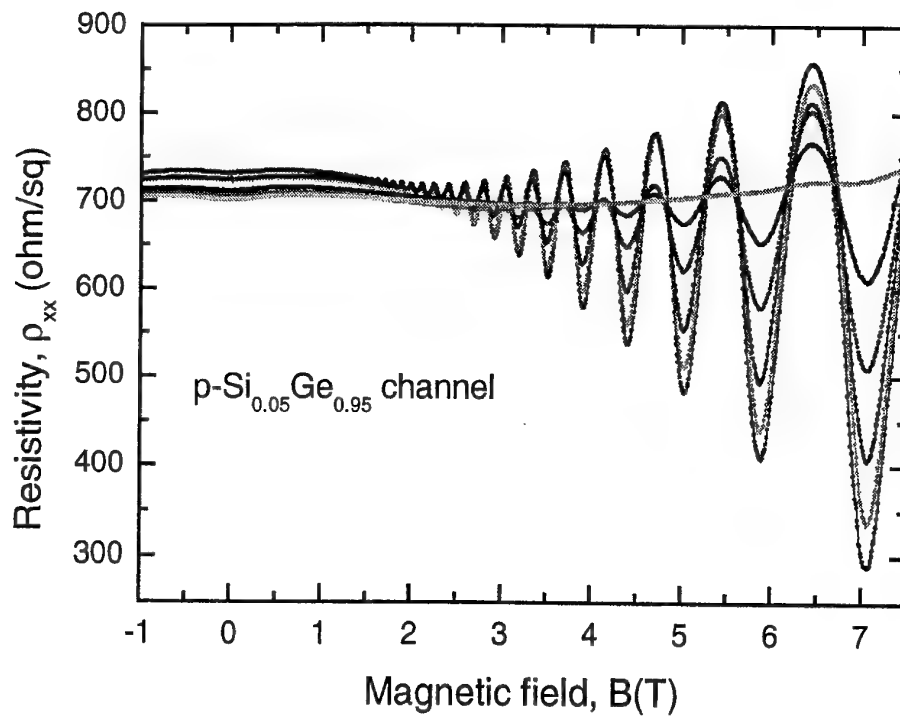


Fig. 1. Magnetic field dependences of longitudinal resistivity  $\rho_{xx}(B)$  measured at temperatures 0.356mK – 20.7K for  $\text{Si}_{0.05}\text{Ge}_{0.95}/\text{Si}_{0.37}\text{Ge}_{0.63}/\text{Si}(001)$  p-type modulation doped heterostructure.

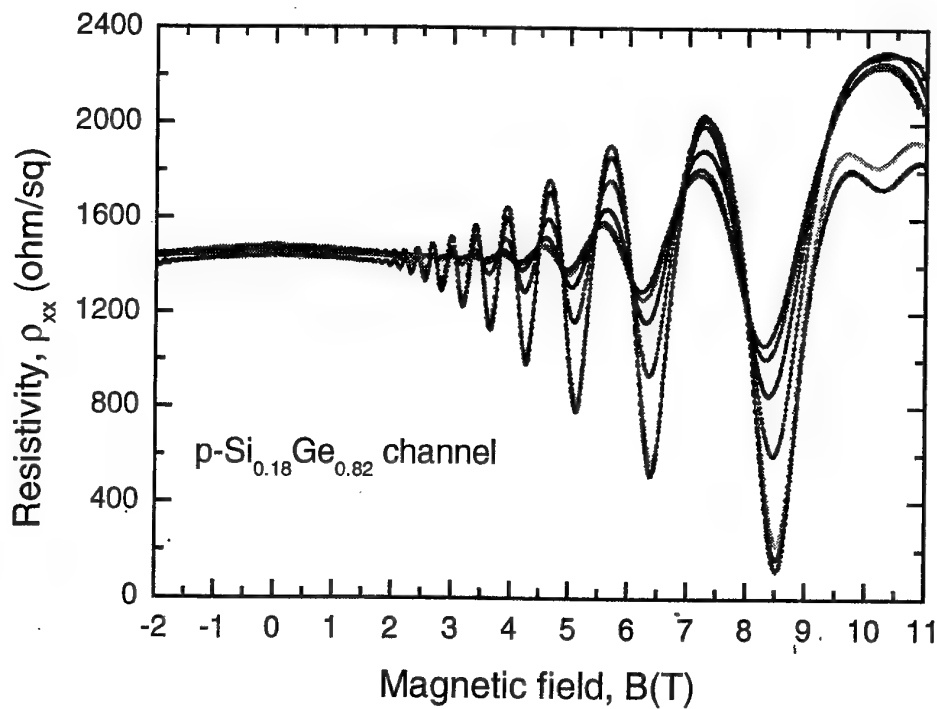


Fig. 2. Magnetic field dependences of longitudinal resistivity  $\rho_{xx}(B)$  measured at temperatures 0.348mK - 8.5K for  $\text{Si}_{0.18}\text{Ge}_{0.82}/\text{Si}_{0.47}\text{Ge}_{0.53}/\text{Si}(001)$  p-type modulation doped heterostructure.

**SESSION C**  
**(invited)**  
**Emerging Technologies**

# Pentacene Organic Thin Film Transistors

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Organic thin film transistors (OTFTs) have made impressive progress over the past decade, and it appears increasingly likely that OTFTs will find use in a variety of low-cost, large-area electronic applications, such as flat-panel displays, chip cards, merchandise tags, and sensor arrays. In contrast to TFTs based on inorganic semiconductors, such as hydrogenated amorphous silicon (a-Si:H), OTFTs can be fabricated using substantially lower process temperatures, with the possibility of utilizing inexpensive substrates of arbitrary size and shape, such as flexible polymeric film or paper. In addition, OTFTs based on polymers may allow extremely efficient printing techniques to be applied to deposit and pattern the materials.

OTFTs have been demonstrated using a wide variety of organic semiconductors, including both polymers and small-molecule materials. To date, the best electrical performance has been obtained with OTFTs based on pentacene as the active material [1]. Pentacene is a short-chain molecule consisting of five linearly fused benzene rings and is typically deposited by thermal evaporation in vacuum, onto substrates held at slightly elevated temperature (60 °C) in order to improve molecular ordering and carrier mobility [2].

Pentacene OTFTs on glass substrates have demonstrated carrier field-effect mobility as large as 1.7 cm<sup>2</sup>/V-s, subthreshold slope as low as 0.4 V/decade, and on/off current ratio larger than 10<sup>8</sup>, making them suitable for low-voltage electronic applications. With pentacene OTFTs fabricated on flexible polyethylene naphthalate (PEN) film, carrier field-effect mobility of 1 cm<sup>2</sup>/V-s, near-zero threshold voltage, and on/off current ratio of 10<sup>7</sup> have been obtained. Integrated circuits based on pentacene OTFTs on PEN film have shown propagation delay below 50 µsec per inverter stage, measured using 5-stage ring oscillators with 8 V power supply. Propagation delay in these circuits is not limited by intrinsic transistor speed, but by parasitic elements due to a non-optimized circuit layout. Directly driven pentacene OTFTs have

demonstrated sub-microsecond switching time constants.

Pentacene OTFTs have also been used to demonstrate several technology coupling scenarios. Although ambipolar carrier transport has been observed in pentacene single-crystals and utilized to demonstrate complementary inverter operation [3], thermally evaporated pentacene is typically useful only as a p-type semiconductor. To evaluate the prospects of an integrated complementary thin film technology for low-power applications, pentacene p-channel OTFTs were integrated with n-channel a-Si:H TFTs on glass substrates [4]. These circuits have propagation delay as low as 5 µsec per stage and power dissipation as low as 0.2 µW per stage, measured using ring-oscillators.

Pentacene OTFTs have also been used to create active emissive pixels in which an organic light emitting device (OLED) is integrated with the channel region of a pentacene OTFT [5]. In these integrated pixels, charge carriers enter the organic emissive layer directly from the pentacene channel, thus eliminating the metal contacts and the metal wiring typically used to connect the drain of the OTFT to the anode of the OLED, while also providing substantially improved carrier injection for the OLED.

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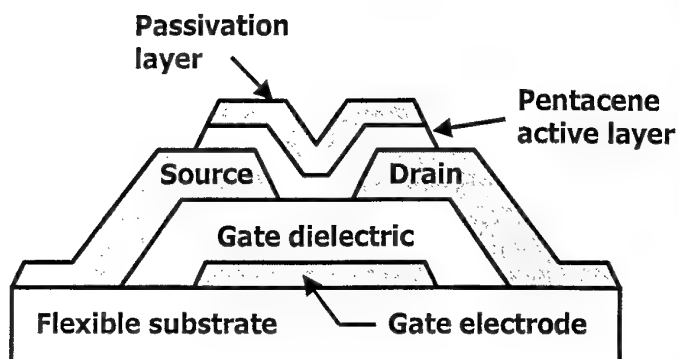


Fig. 1. Cross section of a discrete pentacene OTFT on flexible polyethylene naphthalate (PEN) film.

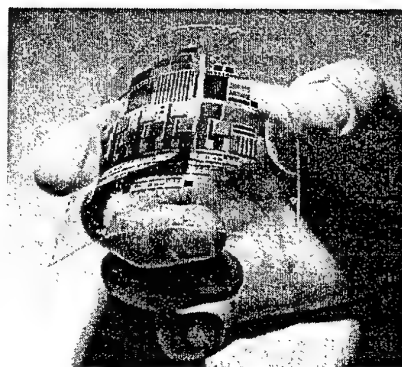


Fig. 2. Flexible PEN chip with pentacene OTFTs and circuits.

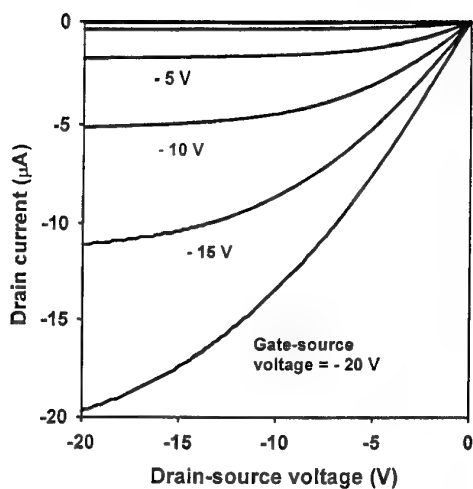


Fig. 3. Electrical characteristics of a pentacene OTFT on PEN film.

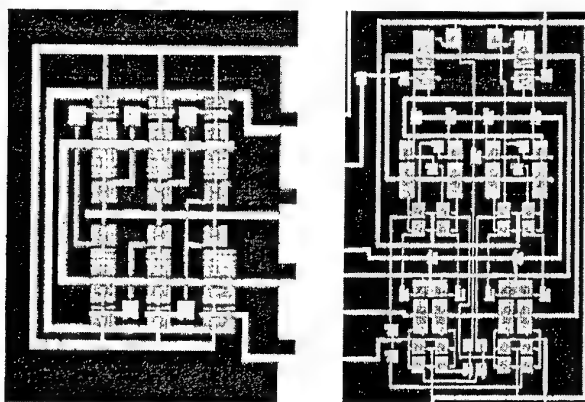


Fig. 4. 5-stage ring oscillator with output buffer (left) and differential amplifier (right) fabricated on flexible PEN film using pentacene OTFTs.

Fig. 5. 5-stage ring oscillator with output buffer in pentacene / a-Si:H complementary thin film technology fabricated on glass.

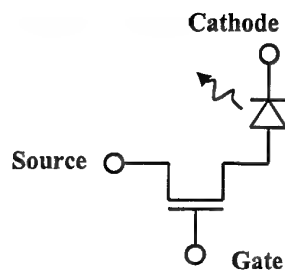
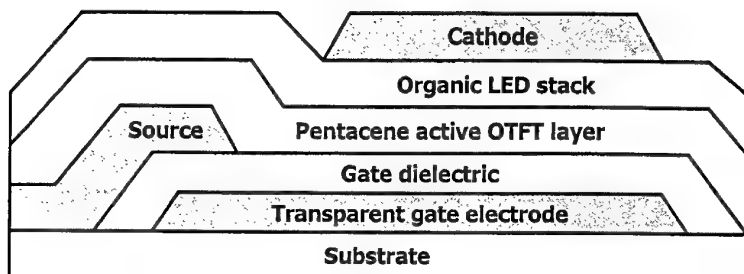
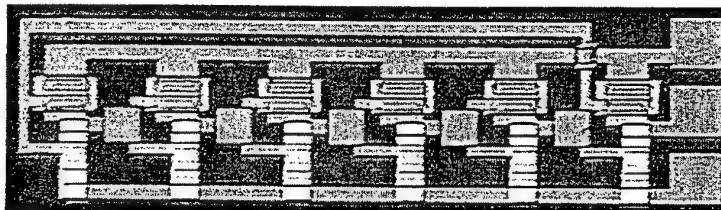


Fig. 6. Schematic cross section and circuit representation of an integrated active emissive pixel.

## **Organic Devices at Nanometer Scale Using Self-Assembled Monolayers**

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Supramolecular assembly of organic molecules on solid substrates (especially on semiconductors) is a powerful "bottom-up" approach for the fabrication of devices for nanoelectronics and molecular-scale electronics.

I will review the main structural and electronic properties of such self-assembled monolayers on silicon and III-V semiconductors and I will describe several applications:

- SAMs in organic and inorganic nanometer-scale FET's
- SAMs to control the electronic properties of semiconductor surfaces
- SAMs as ultra-high resolution e-beam resists
- SAMs as building block for the fabrication and test of unimolecular devices like molecular rectifying diodes, molecular wires, negative differential resistance molecular diodes,...

## **SESSION D**

**D1. III V Sensors**

**D2. Diamond Sensors**

# Technology of Integrated Application Specific GaAs Flow Sensors

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## Abstract

This work reports on the development of GaAs-based anemometers for flow analysis in applications where the magnitude of the flow velocity as well as the direction have to be determined. The developed devices have been designed for integration in the space between the rotor blades and the stator of an axial compressor. Novel material properties, such as strong Seebeck coefficients, high thermal resistivity and selective etching capability, of III-V compound semiconductors and their heterostructures, are used here to define sensitive membrane-based flow sensors [1].

The essential part of this type of sensors is a micromachined sensing area made of a selectively-etched high thermal resistivity layer such as  $\text{Al}_{0.48}\text{Ga}_{0.52}\text{As}$  or  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ . A dc current flowing in an heating resistor heats up the membrane and the temperature difference to the bulk is measured by means of a series of integrated Au-Cr/GaAs thermocouples (Thermopiles) left and right of the resistor. An air flow on the sensor surface cools down the membrane and reduce the temperature gradient, causing a change in the output thermovoltages. In this way flow velocity and direction can be measured by combining the measured thermovoltages left and right the heating resistor. Depending on the application a suspended membrane can also be used. A schematic of the sensor is shown in Fig.1a. The necessity for a planar mounting of the sensor in the stator wall without wire bonding for electrical connections in order to avoid disturbing the flow to be analyzed rises the question of an appropriate connection technology as well as the corresponding packaging strategy. A via-hole technology has been added to the backside process for the electrical connections and a special package developed (Fig. 1b). Typical sensor outputs and direction are shown in Fig. 2. The 2 microns thin membrane structure could sustain the up to 80 mbar pressure difference in the compressor without damage. More work on the packaging aspects, test and reliability of the sensors is still needed to increase the yields and reduce manufacturing costs.

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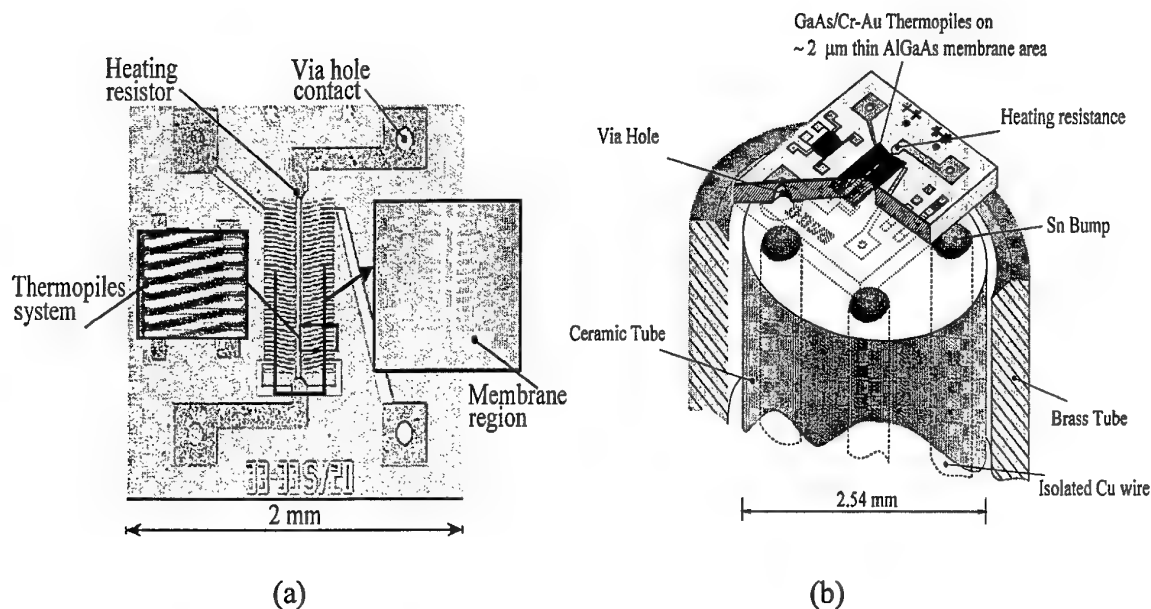


Fig. 1 (a) Top view of a AlGaAs/GaAs gas flow sensor. The thickness of the sensor chip is 150  $\mu\text{m}$ . Cr-Au/GaAs thermocouples are placed in the membrane region on the right and the left of the heating resistor. The membrane thickness is 2  $\mu\text{m}$ . A Via hole technology is used for the electrical connection of the sensor. (b) The shown specific packaging is used for flow analysis in the space (0.9 mm) between the rotor blade and the stator of an axial compressor for turboengines.

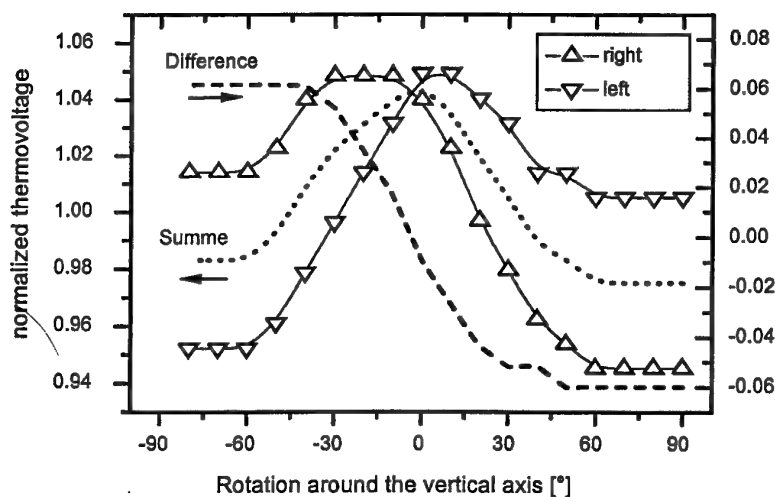


Fig. 2 Typical sensor output for a rotation around the vertical axis

# Concept of a Gyroscope in Hetero-Micromachining

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Juni 30, 2000

## Introduction

A high volume market for low cost and medium performance inertia sensors like accelerometers or gyroscopes is the automotive industry. In the applications like aviation, navigation and industrial measurement (robotics, machine monitoring) a higher performance is required. Hetero-micromachining (HMM) offers the potential of integration of complex electro-mechanical structures and electric circuits in silicon technology.

## Experimental

Angular motion can be measured by exploiting the Coriolis force. A spring-mass resonator is used which is compliant with respect to oscillations in two perpendicular directions. By rotation about an axis perpendicular to these directions both modes of vibration are coupled by Coriolis force.

The design of our composite beam spring-mass resonator is derived from a gyroscope fabricated by Li et al. [1] using bulk micromachining. We use an InP layer as etch mask and as part of the electro-mechanical transducer. Different to conventional bulk micromachining where a second wafer may be necessary (e.g. for electrostatic excitation or capacitive measurement) our concept allows for monolithic integration of actuating and sensing functions on the sensor chip.

Figure 1 shows scanning electron microscope (SEM) micrograph from the backside of a composite beam spring-mass resonator realized in HMM. The first process step is the growth of an epitaxial InP layer on backside-oxidized (001) silicon. The layer thickness is typically around 2.5  $\mu\text{m}$ . Next the  $\text{SiO}_2$  coating is removed completely using HF. The backside oxide is necessary during epitaxy to reduce the incorporation of Si impurities in the InP layer [2].

Subsequently the InP layer is structured using  $\text{HCl}:\text{H}_3\text{PO}_4$  (1:4). Due to the high etch selectivity between InP and Si the latter is used as etch stop in vertical direction. Finally the silicon is etched using KOH solution (30 %; 60 °C).

Because of the anisotropic etching behaviour of Si in KOH, it is possible to realize seismic mass, T-beam and a suspension consisting of InP cantilevers (cf. Fig. 1) in a single etch step. For the definition of the seismic mass the etchstop behaviour of the {111}-crystal planes is used. The structures of the suspension and the T-beam are oriented along  $\langle 100 \rangle$  crystal directions. In this case lateral etching proceeds as fast as in vertical direction leading to a complete removal of the silicon underneath the suspension (lower part of Fig. 1) and the formation of the T-shaped beam between the suspension and the seismic mass.

The suspension is compliant to an oscillation in vertical direction which can be actuated thermally exploiting the different thermal expansion coefficients of InP and Cr/Au metallization as demonstrated in a previous study [3] or by using a piezoelectric actuator. The latter offers the advantage of lower power consumption.

Figure 2 depicts the concept of a piezoelectric actuator which is based on a highly resistive InP layer on top of a conductive bottom layer. Due to diffusion of Si from the substrate into the layer the InP close to the heterointerface is highly n-doped and offers a good conductivity as shown in the measured carrier concentration profile in Fig. 2. We use this part of the layer as backside electrode which is contacted through a viahole etched

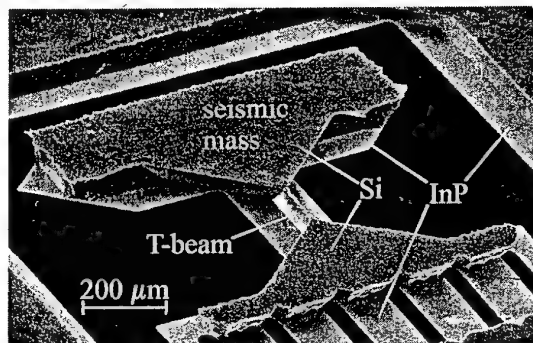


Figure 1: SEM micrograph of a composite beam spring-mass resonator in HMM.

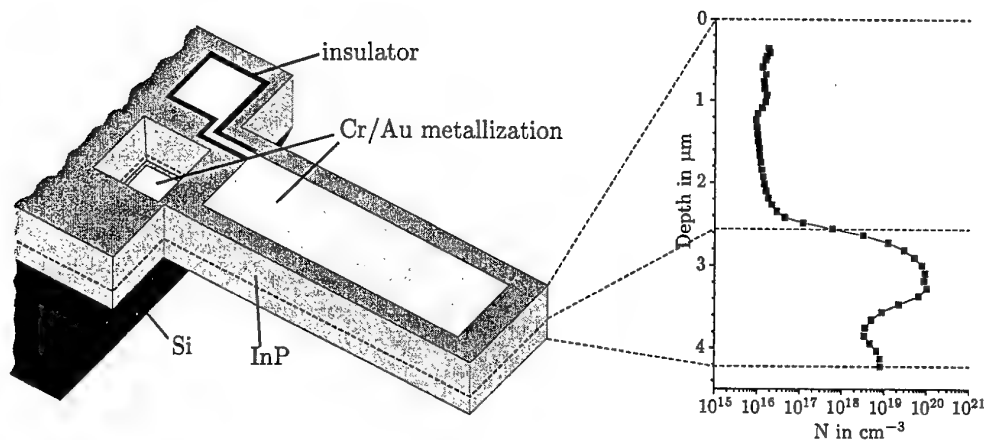


Figure 2: Concept for an actuator in HMM based on a measured electron concentration profile

through the highly resistive part of the InP layer. To avoid leakage currents between the wiring for the frontside electrode and the backside electrode an insulator layer is deposited in the area of the wiring. The Cr/Au metallization in the viahole and for the frontside electrode is deposited by e-beam evaporation and structured by lift-off technique.

## Results and Discussion

The area consumption of the composite beam spring-mass resonator in HMM is about an order of magnitude smaller compared to the gyroscope realized by Li et al. [1]. The eigenfrequencies of this structure still have to be measured.

The concept for the actuator has been realized on test structures of cantilevers that are  $3.5\text{ }\mu\text{m}$  thick,  $250\text{ }\mu\text{m}$  wide and  $1000\text{ }\mu\text{m}$  long. To measure the actuation of our cantilevers a laser beam was focused on the cantilever. The reflected light was detected by with a position-sensitive photodiode. For excitation we use a frequency generator which provided an output voltage of  $10\text{ V}_{\text{eff}}$ . In Fig. 3 the measured actuation is plotted against the excitation frequency. The data points were fitted with the dependency for a forced harmonic oscillation. As a result of this fit we obtained an eigenfrequency of  $2282\text{ Hz}$  and a Q-factor of 229. The theoretical value for the eigenfrequency is  $2445\text{ Hz}$ . The difference is explained by lateral underetching and the limited immunity of InP against KOH solution.

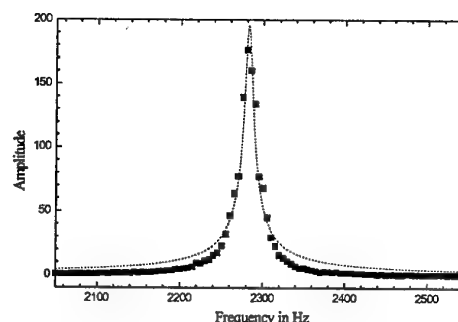


Figure 3: Actuation in dependence of excitation frequency

## Acknowledgements

We are grateful to D. Niemeyer, D. Rümmler, N. Riedel and A. Tiefnig for active technical support in technology and characterization. This work is funded by the Deutsche Forschungsgemeinschaft (DFG).

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# Diamond Electromechanical Relay

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Diamond has been intensively studied in the last years for various purposes including heat sinks, electronic devices and as coating material. Its outstanding properties also predestine the material for MEMS applications. Especially the high hardness, high fracture strength and the high thermal conductivity are desirable properties for microelectromechanical devices. Diamond is also a multi-purpose material which can be insulating, semi- and metal-like conducting, thus avoiding problems normally found in multi-layer device structures, like thermally induced stress or thermal barriers.

In this work an all-diamond microswitch is investigated. The device structure and a SEM picture are shown in figure 1. Details on device technology can be found in [1]. The microswitch is electrostatically actuated by applying a voltage to the gate contact, creating an electric field which bends the free standing cantilever thus closing the signal contact (fig. 1). The use of diamond in this device is predicted to have a couple of advantages. First, the heat generated in the device, especially at the contact tip, is effectively distributed due to the very high thermal conductivity. Second, the use of diamond-diamond tunneling contacts reduces the problems of sticking and oxidation often observed in conventional metal-based microcontacts. Also, wear can be greatly reduced due to the high hardness of the material. The third advantage is the high Young's modulus leading to a higher resonance frequency of the free standing cantilever and therefore higher maximum operation frequency.

The device has been fabricated using a surface-micromachining process [1] and device properties have been investigated by simulation and measurement.

Figure 2 shows the simulated temperature distribution in the switch for a power loss at the contact tip of  $3.2 \text{ MW/cm}^2$ . At this power level, a maximum temperature of approx.  $600^\circ\text{C}$  is observed, which represents the oxidation temperature of diamond in air at which device degradation is expected. Experimentally, a maximum power loss of  $0.74 \text{ MW/cm}^2$  has been measured before destructive contact degradation occurred. The difference is believed to be caused by the nonuniform current distribution over the contact area creating 'hot spots'.

The switching behaviour is shown in figure 3. Experiments in vacuum and air have been carried out, showing a significant increase of the switching time in air due to gas damping [2]. Calculations taking this effect into account can predict the switching time satisfactorily.

First lifetime measurements also show promising results,  $>10^4$  switching events under load ( $J_{\text{signal}}=250 \text{ A/cm}^2$ ) could be measured without destruction of the device. In all experiments, no sticking has been observed.

The results show, that the expected advantages of diamond as MEMS material indeed can be observed in real devices, making it an interesting alternative to currently used materials like silicon or nickel.

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„Performance of High Speed Diamond Microswitch“  
Proc. Micromat 2000, April 2000, Berlin, Germany

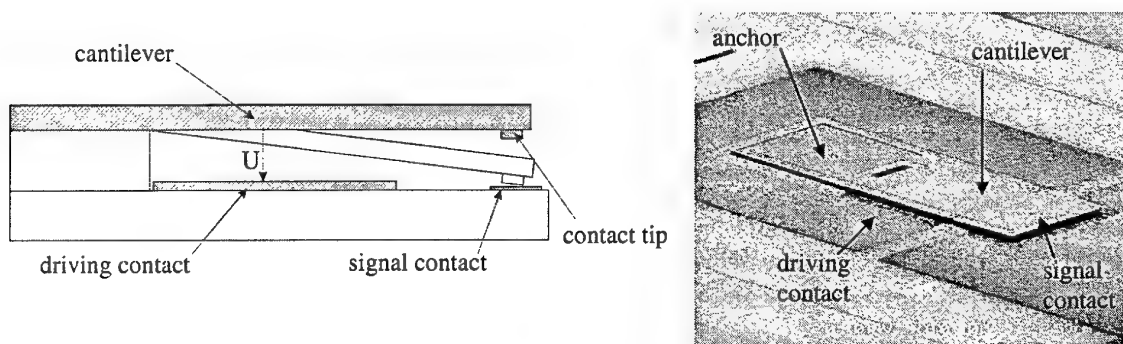


Figure 1: Cross section of all-diamond microswitch (dark: el. conducting diamond, light: insulating diamond) and SEM picture of fabricated device.

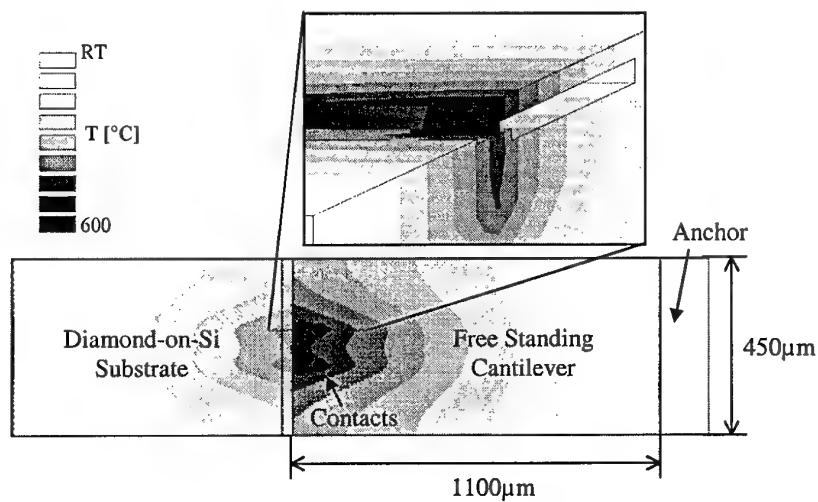


Figure 2: Simulated temperature distribution of microswitch with two contact tips of area  $A=20 \times 20 \mu\text{m}^2$ , power loss at contact  $3.2 \text{ MW/cm}^2$ .

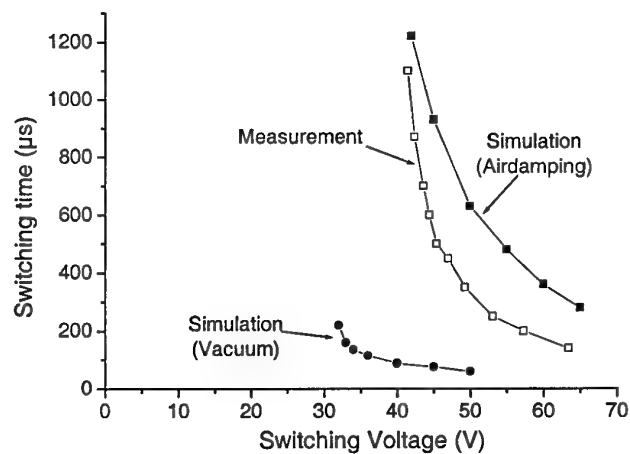


Figure 3: Measured switching time of diamond microswitch compared to simulation results excluding and including air damping effects.

## DIAMOND RADIATION DETECTORS

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Natural diamond was one of the first solids to be considered for possible use as a nuclear radiation detector. The first observation of pulses due to discrete radiations was noted by Stetter [1] in 1941 and then by Wooldridge, Ahearn, Friedman and Hofstadter. But the counting properties were uncontrollable (depending on the crystal and type of radiation). Moreover the charge polarisation leads to reduction in counting rate and pulse amplitude as a function of the time of irradiation. Due to these dysfunctions and progress in Ge and Si, diamond was not studied so intensively. Wouters and Christian (1947) and Mc Kay (1950) used an accelerating field to suppress the effect of polarisation. Later in 1951 Chynoweth reduced polarisation by illumination with red light. In 1959 diamond was tested by Kennedy with high-energy electrons and by Champion and Wright with alpha particles. Dean and Male measured the detection efficiency of  $\beta$  and  $\alpha$  particles in 1964. In 1975 Kozlov published the electric and detection characteristics of natural diamond counters and also possible applications (mainly space ones) were discussed [2]. In 1981 Burgemeister reported nature diamond as a detector for radiation measurement in medical field.

Because of the high cost and difficulties in selecting natural diamond gems of suitable quality, diamond has not found general applications in the fields of particle detection until the CVD (Chemical Vapor Deposition) technology was developed in 1981 [3]. This technology allows a low cost diamond production in large sheets and with higher purity than nature diamonds. CVD diamond is a resilient material with excellent physical properties for radiation experiments. Its high radiation hardness makes it an ideal material, especially in the high radiation environments of future colliders, such as the LHC (Large Hadron Collider) in CERN or in any another hostile radiation environments in which more conventional detectors (like Si or Ge det.) would fail. Except radiation hardness diamond is able to survive a harsh thermal and chemically aggressive environment. The absorption characteristics of CVD diamond are well matched to human soft tissue, so that diamond ( $Z=6$ ) can be considered soft-tissue-equivalent ( $Z=7.42$ ). This diamond property is very important for radiation dosimetry applications especially for medical ones. Low atomic number of diamond results in a low X-ray absorption and allows using of diamond for on-line X-ray flux measurements. CVD diamond was also used as a material for real time beam position monitor, which has achieved excellent position sensitivity [4].

There have been prepared generally four types of CVD diamond detectors: coaxial, planar, micro-strip and pixel detectors.

By **coaxial micro detectors** the diamond film is deposited by hot filament technique on metallic (W, Mo) wires and tips. Tips are obtained by electrochemical etching. CVD diamond film (10  $\mu\text{m}$ ) uniformly covers the W tip and acts as a semiconductor region for X-ray detection. The graphite layer, which covers the

diamond layer, acts as an electrode together with W tip which is grounded. Coaxial micro detector can be used for monitoring X-rays and  $\gamma$ -rays in medical and health physics fields [5]. Coaxial geometry is suitable for miniaturisation of probes. The probes diameter can decrease up to 50  $\mu\text{m}$ . This kind of probes is suitable for "in vivo" dosimetry, X-ray profiling and in small-diameter radio surgery beams.

**Diamond detectors prepared in CERN (RD42)** have been studied as particles paths trackers. There have been investigated micro-strip and pixel diamond detectors [6].

Micro-strip detectors have on irradiating side of diamond a pattern of strips (50  $\mu\text{m}$  pitch). The other surface of diamond is covered by uniform metal contact. It has been used chromium covered by gold to produce ohmic contact. The thickness of a diamond layer for detector applications is typically around 500  $\mu\text{m}$ .

Pixel detectors, unlike strip detectors, are able to track the particle path in both directions of plain. The pixel cells of metallization pattern are made with Cr-Au contacts with size of 100\*100  $\mu\text{m}^2$ . The gaps between metallized squares are 50  $\mu\text{m}$ .

The polycrystalline diamond films for **planar detectors** were deposited on low resistivity silicon wafers. Gold pads 1 mm in diameter were deposited on the diamond surface to form the electrical contacts. The studies have shown, that CVD diamond planar detectors can be used for alpha particle counting, for characterization of ultra fast ( $\sim 100\text{ps}$ ) laser pulses and for X-ray flux and dose measurements [7]. CVD diamond was also studied as a material for  $\gamma$ -dose rate monitor for high radiation environment [8].

Recently, diamond layers technology has been successfully applied also at Slovak University of Technology [9]. In collaboration of Department of Microelectronics and our Department of Nuclear Physics and Technology the first diamond layers for detection of ionising radiation were prepared by CVD technology. These diamond structures were tested by alpha particles from  $^{241}\text{Am}$  source (5.49 MeV).

## References:

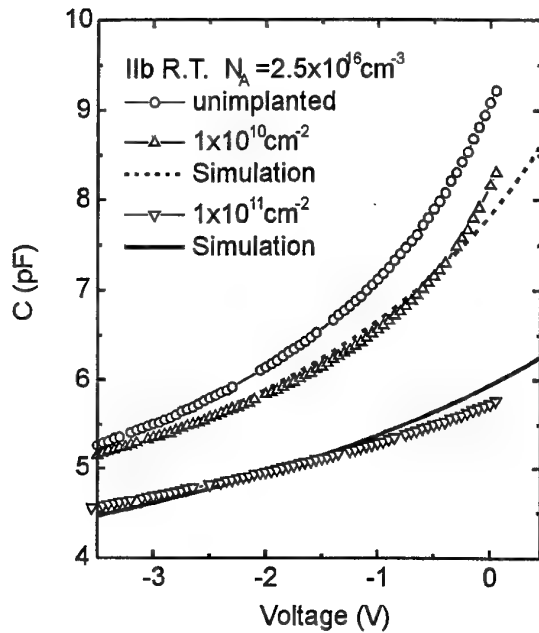
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# Characterisation of radiation damage in type IIb diamond by capacitance techniques

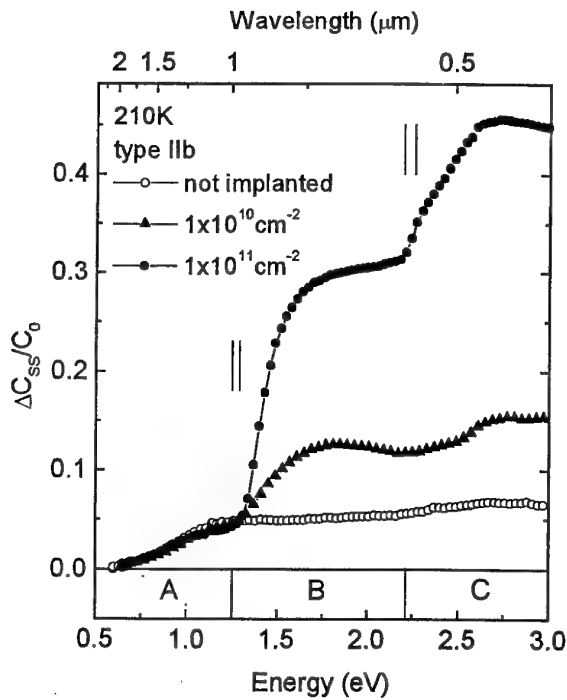
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Due to its outstanding properties, diamond is a promising material for UV and particle detectors in harsh environments. In spite of its high radiation hardness, even diamond suffers from radiation damage induced by high energetic particles. In the present paper, we investigate carbon ion implanted type IIb diamonds by means of capacitance techniques. To induce the radiation damage, we used 160 keV  $C^+$  ions with doses between  $1 \times 10^{10} \text{ cm}^{-2}$  and  $1.1 \times 10^{11} \text{ cm}^{-2}$ . These doses were chosen to keep the defect density created by radiation below the boron concentration, which is in our samples  $2 \times 10^{16} \text{ cm}^{-3}$ . This ensured that the p-type character of the diamond is conserved after implantation. Ag Schottky contacts were fabricated on the implanted as well as on reference samples and were characterized by capacitance voltage profiling and optical induced deep level transient spectroscopy (ODLTS). The capacitance-voltage (C-V) characteristics of the implanted samples show a strong dependence of the implantation dose, deviating stronger from an ideal C-V behaviour the higher the dose. This is explained by a model assuming a compensated layer in the radiation damaged volume whose compensation ratio increases with implantation dose. From this fit we calculate the residual boron acceptor density. Optically induced deep level transient spectroscopy (ODLTS) is used to study the radiation induced deep levels. In two spectral regions the absorption is enhanced by ion implantation, namely  $1.3 \text{ eV} \leq h\nu \leq 2.25 \text{ eV}$  and  $2.25 \text{ eV} \leq h\nu \leq 3 \text{ eV}$ . The comparison of the absolute defect densities with the residual acceptor densities leads to the conclusion that the defects causing the absorption in the first spectral region are responsible for the compensation of the boron acceptor.



**Fig. 1** : C-V characteristics of the type IIb diamond before and after carbon ion implantation with various doses. The higher the dose, the more the C-V characteristic deviates from an ideal behaviour. The solid lines represent the best fit to the data after a model accounting for the compensation of the acceptors in the radiation damaged volume



**Fig. 2** : ODLTS signal for implanted and unimplanted type IIb diamond. Here  $\Delta C_{SS}/C_0$  has been evaluated, representing the trap density.

## POSTER SESSION

# Post-growth annealing effect on magneto-transport and structural properties of $\text{Si}_{0.2}\text{Ge}_{0.8}/\text{Si}_{0.65}\text{Ge}_{0.35}/\text{Si}(001)$ modulation doped heterostructure

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The growth of high-quality  $\text{Si}_{1-x}\text{Ge}_x$  epilayers with  $x > 0.5$  on Si substrate by molecular beam epitaxy (MBE) is of great interest both for device applications and fundamental research. The main problem in growing  $\text{Si}_{1-x}\text{Ge}_x$  alloy on a Si substrate is the lattice mismatch, which increases from 0 to 4.2% as  $x$  is varied from 0 to 1. The larger  $x$  becomes, the thinner the  $\text{Si}_{1-x}\text{Ge}_x$  channel has to be grown in order to prevent misfit dislocations from relaxing the strain. One of the possibilities to obtain Ge compositions  $x > 0.5$ , while retaining strain in the  $\text{Si}_{1-x}\text{Ge}_x$  layer, is to use relaxed  $\text{Si}_{1-y}\text{Ge}_y$  substrate with the bulk lattice constant of the  $\text{Si}_{1-y}\text{Ge}_y$ . This allows either strained Si, Ge or  $\text{Si}_{1-x}\text{Ge}_x$  to be grown on an underlying Si wafer. Such substrates are termed virtual substrates (VS).

The magneto-transport and structural properties of  $\text{Si}_{1-x}\text{Ge}_x/\text{Si}_{1-y}\text{Ge}_y/\text{Si}(001)$  p-type modulation doped heterostructure grown by a combination of solid source MBE and low pressure CVD on Si(001) are reported. The Ge composition in the channel and VS of as-grown sample is 0.8 and 0.35 respectively. The heterostructure was grown at relatively low temperature to avoid strain induced roughening of the channel. To improve the magneto-transport characteristics of grown structure furnace thermal annealing treatments were performed, following growth, in nitrogen atmosphere in the temperature range of 600-750°C for 30min.

Cross-sectional TEM was performed on as-grown and annealed samples to determine the structural integrity of the epilayers and also to determine the dislocations microstructure in relaxed virtual substrate. In all annealed samples, we observed broadening of the  $\text{Si}_{1-x}\text{Ge}_x$  channel, accompanied by a reduction of the Ge content from 0.8 for the as-grown sample to 0.66 for the 750°C annealed sample. In addition, high resolution x-ray diffraction investigations were performed on the as-grown and annealed samples. From the scattered intensity distribution in reciprocal space maps recorded around the (004) and (224) reciprocal lattice points, the strain gradient in the  $\text{Si}_{1-y}\text{Ge}_y$  buffer layers and the in-plane strain values of the  $\text{Si}_{1-x}\text{Ge}_x$  channels were determined. For the latter, typical values are  $\epsilon_{||} = 1.93 \cdot 10^{-2}$  for the as-grown sample and  $\epsilon_{||} = 1.28 \cdot 10^{-2}$  for the sample annealed at 750 °C.

The mobility and sheet carrier density of as-grown and annealed samples were obtained by a combination of resistivity and Hall effect measurements ("Van der Pauw" sample geometry) in the temperature range of 9-300K. The annealing at 600°C is seen to have a negligible effect on the mobility. Increasing the annealing temperature results in pronounced successive increases of mobility. A moderate decrease of the sheet carrier density with annealing is observed. The best low temperature mobility in this research was obtained after thermal annealing at 700°C. At 9K we observed an increase of mobility (at sheet carrier density) from  $655 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1} (1.43 \cdot 10^{12} \text{ cm}^{-2})$ , in an as-grown sample, up to  $1930 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1} (8.8 \cdot 10^{11} \text{ cm}^{-2})$  in annealed one.

# Dry etching for gate recessing on AlGaIn/GaN HEMTs

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AlGaIn/GaN High Electron Mobility Transistors (HEMTs) are useful for devices operating under high power, high frequency and high temperature conditions due to large sheet carrier density, small gate leakage and large breakdown voltage. The study of Schottky contacts has a great importance for these applications. To minimise the parasitic source resistances and improve the transconductance, a recessed gate process has been applied for AlGaIn/GaN HEMTs.

GaN and AlGaIn materials are chemically stable and are acid-proof at room temperature. GaN material is slowly etched in hot alkalis and can also be etched electrolytically in NaOH [1], [2]. With such difficulties in obtaining reliable wet etching processes, it is therefore imperative to investigate the dry etching characteristics of these materials.

However, a key factor in developing etch processes for III-nitride materials is the ability to have a selectivity of one material over another (GaN, the doped cap layer, over AlGaIn, the Schottky barrier, in our case).

We decided to work on the reactive ion etching (RIE) characteristics of GaN and AlGaIn in SiCl<sub>4</sub> plasma at 20 mTorr [3].

The GaN and AlGaIn (15% of Al content) samples used in this study were epitaxially grown by MOCVD on sapphire substrates.

For etch rate determination, the samples were patterned with a thick electronic resists mask used for gate realization. The etched depths were measured using a Tencor profilometer.

We have observed that, whatever the rf power used AlGaIn material was etched slightly faster than GaN material. Then, we have determined the experimental conditions to only etch AlGaIn material by reducing the rf power. Moreover, it is well known that a dry etching damages the surface. By decreasing the rf power, we reduce these damages. Then, the etched depth control is better.

Moreover, the etching of electronic resists is low and its profile is not damaged. So, we could process a gate recess with a short gate length.

But, we would prefer to etch the GaN material without etching the AlGaIn material. To avoid this problem, we propose a new structure which permits to realize a recessed gate process (figure 2).

Thus, we could totally etch the AlGaIn cap layer. The etch rate would strongly decrease in the GaN layer and the etching would stop just under the interface GaN-AlGaIn (on the Schottky barrier).

A such process would permit to increase the doping level of the AlGaIn cap layer to improve the ohmic contacts without spoiling electrical properties of the Schottky contact.

In summary, we began to study a process which would allow to realize a recessed gate on AlGaIn/GaN HEMTs [4] using dry etching. As the AlGaIn etch rate is higher than the GaN etch rate, we propose a new structure of device.

## Acknowledgments

This work was carried out with the financial help of the DGA (French Army), Contract N° 97-065.

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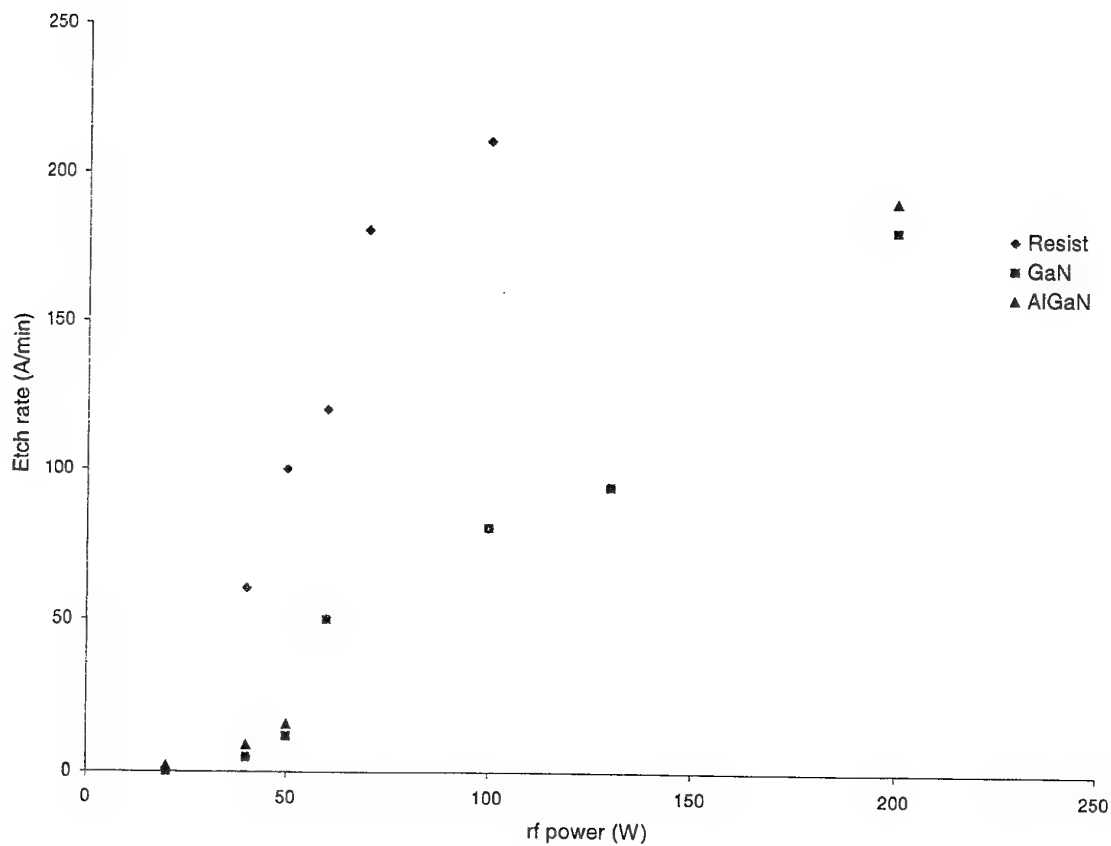


Figure 1

AlGaN doped with Si (cap layer)
GaN
AlGaN undoped (Schottky barrier)
GaN (channel)
Sapphire substrate

Figure 2

# HIGH POWER TIME DOMAIN MEASUREMENT SYSTEM WITH ACTIVE HARMONIC LOAD-PULL FOR BASE STATION AMPLIFIER DESIGN

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## ABSTRACT

A measurement system combining vector corrected waveform measurements with active harmonic load-pull extends, for the first time, real-time experimental waveform engineering up to the 30W power level.

## INTRODUCTION

At the present time, a key design challenge is the realization of linear and efficient high power amplifiers for the next generation of mobile communication base stations. It is the theoretical analysis of terminal voltage and current waveforms that provides a clear understanding of amplifier modes of operation required for high linearity, efficiency and power [1,2]. Hence, the experimental measurement, analysis, and engineering of waveforms should be the preferred method of choice when optimizing (tuning) amplifier performance. However, commercially available systems do not provide any waveform information, resulting in time-consuming device optimisations where the harmonic loads are varied randomly. In this paper a measurement system is demonstrated, for the first time, that allows for waveform measurements, and analysis, combined with real-time waveform engineering utilizing an active harmonic load-pull. Real-time waveform engineering on a commercially available 4W LDMOS transistor is performed to demonstrate how most advantageous the waveform-based approach is for device optimization.

## SYSTEM DESCRIPTION

The system is based on a two channel sampling oscilloscope and test set, with a similar structure to that presented in [3]. Figure 1 depicts the block diagram of the developed high power system. Time domain high power testing capabilities and active load-pull involving three harmonics are integrated in the same test bench. Vector corrected time-domain measurements, e.g. current and voltage waveforms, as well as frequency-domain measurements, e.g. S-parameters, for signals between 0.5 and 12.5GHz can be performed. Both the drive stage and the first harmonic load-pull include 200W amplifiers and so far the system was used to test and load-pull packaged devices of up to 30W output power.

## WAVEFORM ENGINEERING

A conventional fundamental frequency load pull analysis requires the measurement of the device at typically few hundred fundamental loads. The harmonic loads are set to a fixed value. Expanding this

optimization approach for multiple loads at higher harmonic frequencies is prohibitive since it requires the measurement of the device at all possible load combinations, for instance the optimization of a device for the first 3 harmonics with 200 different loads at each harmonic results in  $200^3 = 0.2$  million measurements.

The novel optimization approach, presented in this paper, is significantly reducing the amount of measurements. As a result the device under test can be readily optimized for multiple harmonic loads. The new approach is based on real-time waveform engineering. That is, the measured current and voltage waveforms are manipulated by the active harmonic load-pull and the introduced waveform changes are displayed in real-time. The real-time feedback allows for the successive re-shaping of the waveform based on the latest waveform measurements. Hence, the shaping of the waveform is now directed by the waveforms themselves eliminating the random search for optimum loads. For instance, the current and voltage waveforms can be changed in order to reduce their overlap or to increase their peak values thus reducing the dissipated power or increasing the output power, respectively. This optimization approach is demonstrated in Figure 2 on a packaged 4W LDMOS device, where the current and voltage waveforms before and after waveform engineering are shown. The waveforms in the top graph have been obtained through a conventional fundamental load-pull optimization, which has been waveform engineered for maximum output power. The resulted waveforms are shown in the bottom graph. Squaring the voltage wave while maintaining its peak-to-peak value, therefore increasing the fundamental component of the waveform, and broadening the current peak resulted in an output power increase of 20% giving an output power  $P_{OUT}=4.71W$  at the -1 dB compression point. Since the overlap between the waveforms has not changed the drain efficiency of 59.5% could be maintained.

## CONCLUSIONS

A time domain waveform measurement system has been developed that operates at high power levels (up to 30W at present) hence it can be used to evaluate devices at power levels consistent with telecommunication applications. In addition, the integration of this system with harmonic load-pull also operating at these high power levels means that experimental waveform engineering can be used to determine optimum fundamental and harmonic load impedances.

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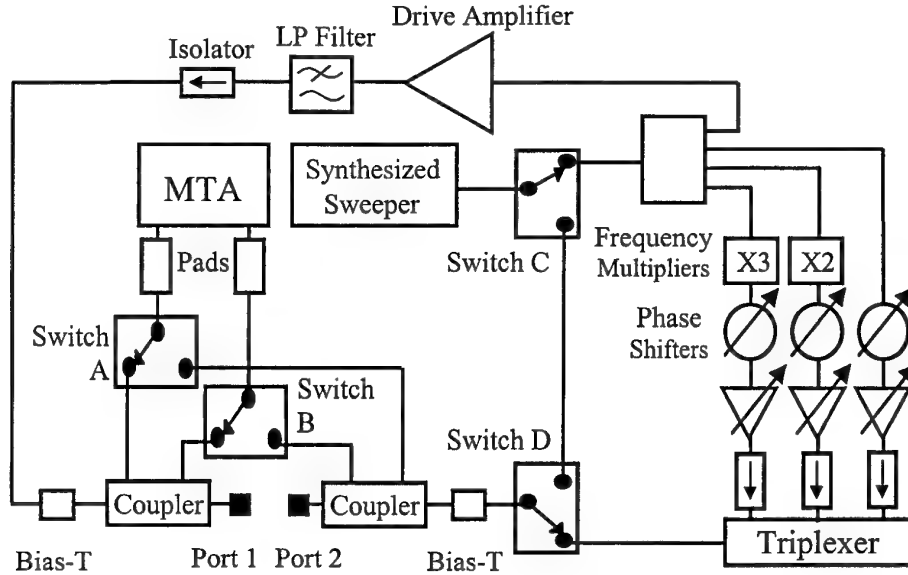


Figure 1: Measurement system schematic

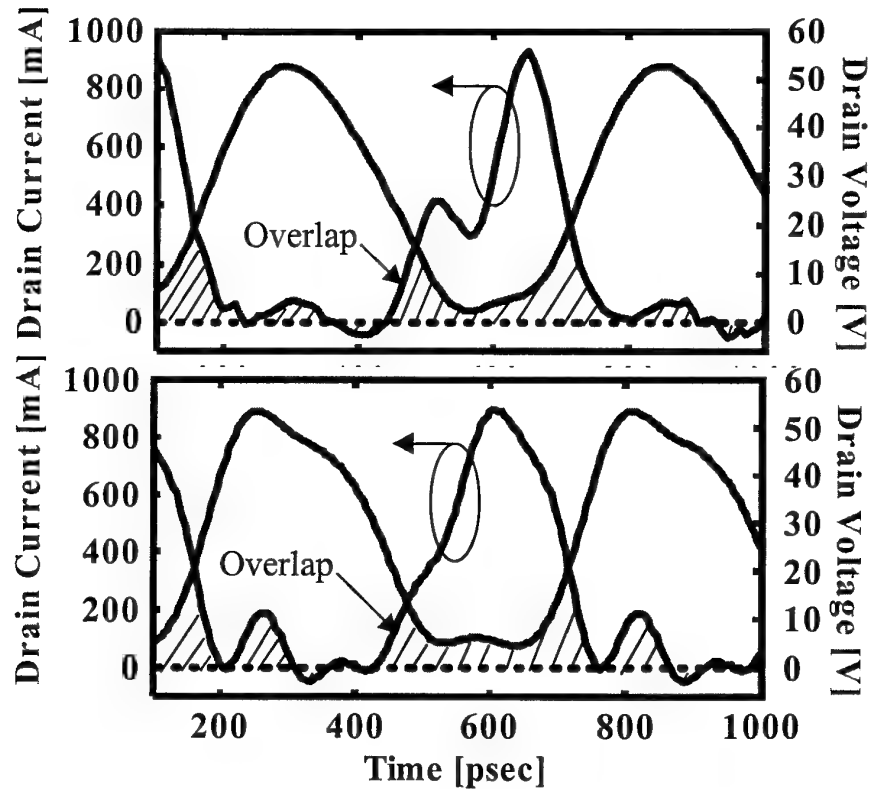


Figure 2: Measured waveforms at the output current generator before (top graph) and after (bottom graph) waveform engineering.

## Low Temperature GaAs micromachined membranes as support for MMIC passive elements

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An alternative solution to the limitation of millimeter wave circuit performance due to the substrate (high dielectric and radiative losses, dispersion effects) is the employment of micromachining techniques. Antennas, filters and transmission lines can be integrated on thin dielectric membranes. For the millimeter wave range it is difficult to integrate the micromachined passive circuit elements manufactured on dielectric membranes on high resistivity silicon with the active devices manufactured on GaAs or other III-V substrates. The GaAs semiconductor membrane as support for microwave circuits represents an interesting solution due to the possibility of integration of passive elements with active elements manufactured on the same substrate. There are two methods for bulk micromachining of GaAs in order to obtain membranes and cantilevers. One method is the nonselective etching, based on isotropic etching of bulk GaAs; 10-25 $\mu$ m thin GaAs membranes can be manufactured. The other method uses selective etching, with  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  as effective etch-stop layer. Heteroepitaxial layers of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  on GaAs with controllable fraction of x can be grown by means of MBE or MOCVD.

In our work conventional and Low Temperature MBE growth of III-V materials was used to fabricate the GaAs/AlGaAs heterostructure presented in Fig. 1. The L.T. GaAs was used because it possesses high resistivity ( $10^6 - 10^7 \Omega\text{cm}$ ). The AlGaAs layer was used as the etch-stop.

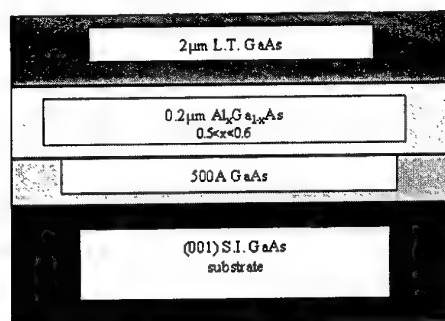


Fig. 1: The GaAs/AlGaAs heterostructure

Conventional contact lithography, e-gun evaporation and lift-off techniques were used to define the filter structure. The membrane etching pattern was defined by backside alignment contact photolithography. The membranes were fabricated by RIE using  $\text{CCl}_2\text{F}_2$  under the following conditions: power: 75mW, background pressure:  $< 5 \times 10^{-5}$  Torr, process pressure: 75 mTorr. End point detection and optical detection was used during the RIE etching.

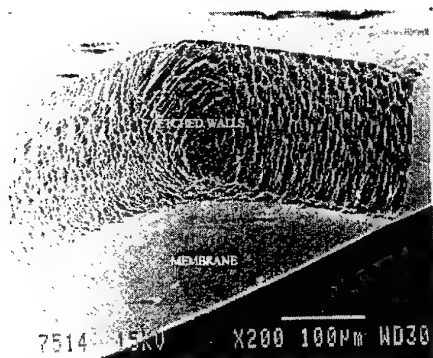


Fig. 2: Etched walls of the structure

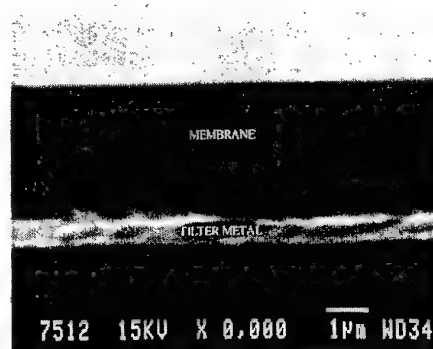


Fig. 3: SEM photo of the membrane, detail

The band-pass filter for 38GHz is based on a four cascaded/opposed double folded CPW open-end series stubs structure. Quarter wavelength folded stubs are used to decrease the length of the filter. The 77GHz filter is based on four cascaded standard CPW open-end series stubs, due to the lower length of the quarter wavelength stubs.

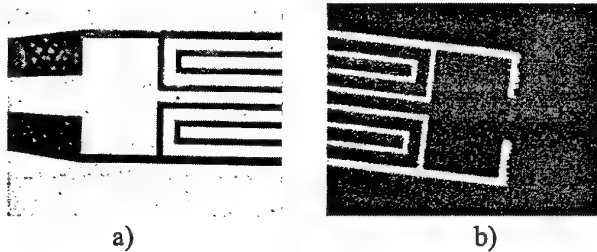


Fig. 4: Photos of the 38GHz CPW filter on GaAs/AlGaAs membrane, patterned by lift-off technique: (a) top view, (b) bottom view.

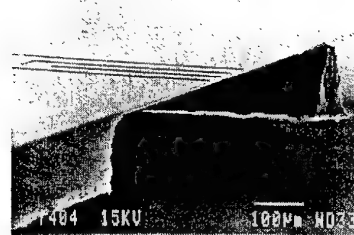


Fig. 5: SEM photo of the 77GHz band-pass filter supported on thin GaAs/AlGaAs membrane manufactured by RIE processed semi-insulating GaAs wafer.

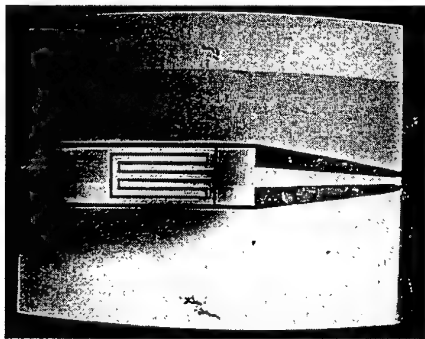


Fig. 6: Detail of the 38GHz 4-cell opposed open-end series stub CPW filter structure supported on a 2.2 µm GaAs/AlGaAs membrane

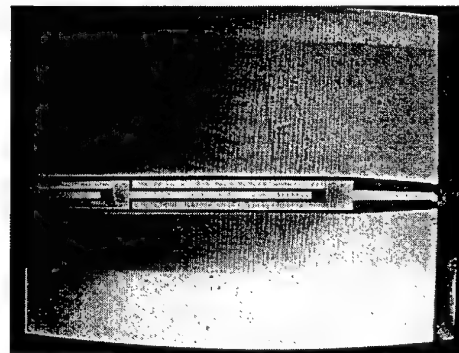


Fig. 7: Detail of the 77GHz 4-cell cascaded open-end series stub CPW filter structure.

The microwave measurements were performed using a on-wafer measuring set-up equipped with Cascade Microtech coplanar probes (with working frequency ranges of 0-50 GHz and 70-110 GHz, respectively) and HP 8510 network analyzer.

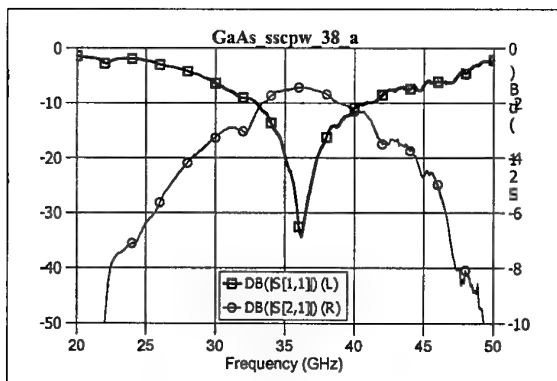


Fig. 8: Measurement results for the 38GHz opposed open-end series stub CPW filter.

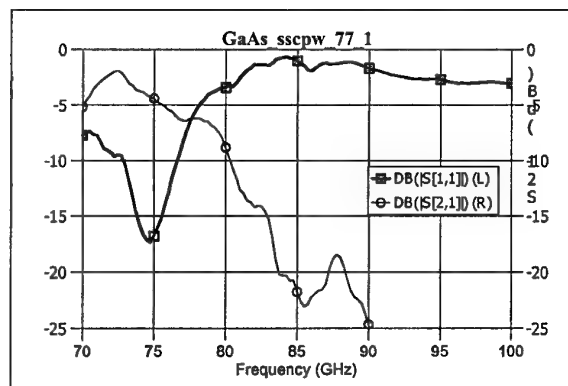


Fig. 9: S parameters measurement for the 77GHz cascaded open-end series stub CPW filter.

Micromachined passive circuit millimeter wave elements (filters for 38 and 77 GHz) supported on GaAs membranes are presented for the first time. Very low losses at 38 and 77 GHz were obtained.

# **A Novel Mobility Spectrum Maximum Entropy Approach for Magnetotransport Analysis of SiGe/Si heterostructures**

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The results of 350 mK - 300 K magnetotransport measurements in static magnetic fields up to 11T are reported for low (pseudomorphic) and high (on virtual substrates) Ge content channels of modulation-doped p-SiGe/(001)Si heterostructures with 2DHG , grown by SS-MBE. With the help of newly developed mobility spectrum analysis technique [1] carrier density and mobility of (i) 2DHG carriers, (ii) boron-supply carriers, and (iii) electron-like carriers are obtained.

The technique utilises the magnetic-field dependence of resistivity tensor and give us spectra, which encode the information about holes constant-energy surface in the strained SiGe channel. A relationship between the mobility spectrum and this sophisticated by strain surface, and a possibility to calculate the drift mobility, Hall mobility, and Hall scattering factor, are discussed.

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## **SESSION E**

**E1. GaN HEMTs**

**E2. GaN Device Technology**

## GaN High Power High Temperature Devices

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Recent achievements in the development of AlGaIn/GaN heterostructure field effect transistors (HFETs) show the great potential for high power and high temperature electronics. GaN based microwave power transistors have set the state of the art for output power density and have the potential to replace other technologies for a number of high power applications [1]. GaN and related heterostructures exhibit attractive electronic material properties such as high breakdown field, modulation doping with high electron mobility and high saturation velocity. These properties facilitate novel high power and high temperature devices that may even beat out competing wide band gap materials.

This paper concentrates on technology and characterization of high power and high temperature AlGaIn/GaN HFETs fabricated at the FBH Berlin. The work comprises GaN HFET process development with a special emphasis to the particular requirements of high temperature and high power operation. The (Al)GaN epilayers used for our investigations were grown by metal organic vapor phase epitaxy (MOVPE) on c-plane sapphire. The growth started with a 2.8  $\mu\text{m}$  thick semi insulating GaN buffer layer followed by a 3 nm  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$  spacer, a 12 nm thick Si doped  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$  supply layer ( $n = 1 \times 10^{19} \text{ cm}^{-3}$ ), a 10 nm  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$  barrier layer and finally a 5 nm thick GaN cap layer. Power HEMT fabrication was carried out with i-line stepper lithography (Nikon NSR-2005i10C) on 2-inch wafers. A special reticle design comprising scaled HFET power cells with different finger dimensions has been applied to optimise power cells with respect to the thermal limitations of the sapphire substrate.

In the first processing step the ohmic source and drain contacts were fabricated using e-beam evaporated Ti/Al/Ti/Au capped with a DC magnetron sputtered  $\text{WSiN}_x$  barrier layer. After RTA at 850°C the ohmic contact resistance was determined to 0.5...0.7  $\Omega\text{mm}$ . Due to the different deposition geometry of metal evaporation and metal sputtering the  $\text{WSiN}_x$  layer totally encapsulates the ohmic contacts. This results in a smooth morphology and well defined contact edges after RTA. A schematic cross section of the active device is given in Figure 1. Aging experiments up to 500°C demonstrated thermal stability of both, electrical performance and contact morphology [2]. Device isolation has been done by reactive ion etching (RIE,  $\text{BCl}_3/\text{Cl}_2/\text{Ar}$ ). Pt/Ti/Au is the standard gate metallization, Ir/Au has been developed for high temperature stable gates. To realize multi finger AlGaIn/GaN-HFETs 3.5  $\mu\text{m}$  thick galvanic air bridges connect the source regions of the individual transistor fingers (see Figure 2).

Reliable high temperature HFET operation calls for a special ohmic and Schottky contact technology. For ohmic contacts the encapsulation technology turned out to be very successful. Stable high temperature Schottky contacts are feasible by using  $\text{WSiN}_x/\text{Au}$  and Ir/Au metallizations. However there is significant advantage of Ir/Au contacts since their room temperature and high temperature barrier height is much higher (about 1.1 eV at RT)) as compared to  $\text{WSiN}_x/\text{Au}$  thus yielding remarkably lower reverse leakage currents. Figure 3 compares the electrical properties of these contacts for temperatures up to 400°C.

Figures 4 and 5 depict the microwave properties of devices with 0.5  $\mu\text{m}$  gate design rule. The current gain cut off frequency  $f_T$  and the maximum frequency of oscillation  $f_{\text{max}}$  are 29 GHz and 60 GHz respectively for a dual-finger transistor. According to Figure 5 calculations using the standard small signal equivalent circuit model indicate very good agreement between the measured and the calculated data.

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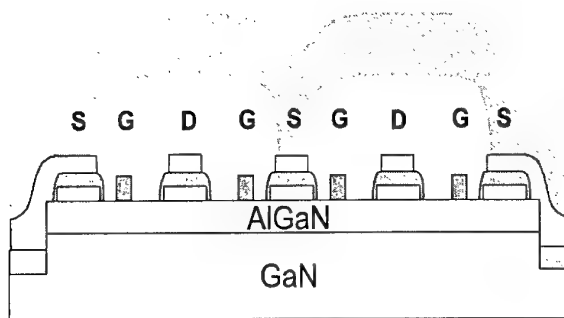


Figure 1: Schematic cross section of a GaN/AlGaN HFET device using ohmic contact encapsulation technique.

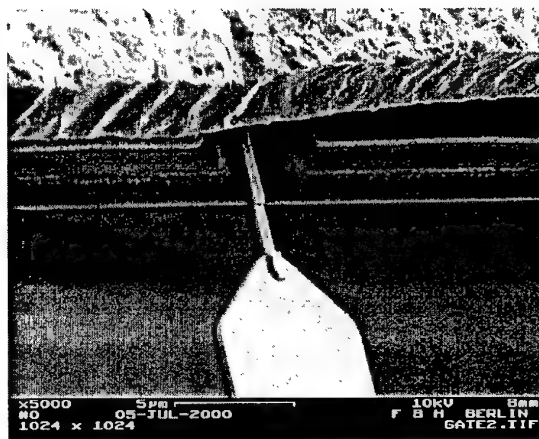


Figure 2: SEM detail image showing the source airbridge, the encapsulated source and drain region and the gate electrode (0.5  $\mu\text{m}$  gate length).

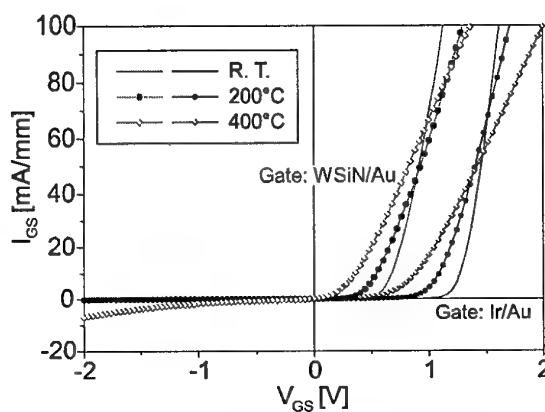
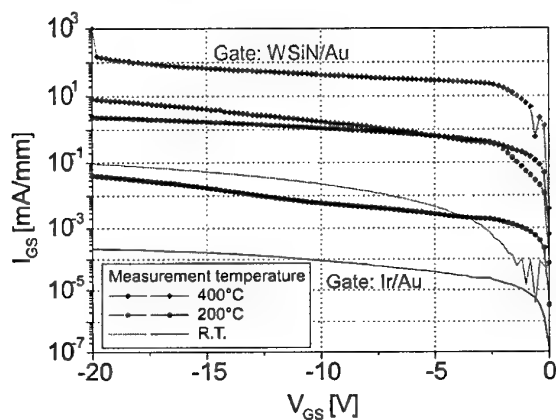


Figure 3: Comparison of high temperature properties of different gate metallizations at different temperatures: (room temperature, 200°C and 400°C), left: reverse characteristics, right: forward characteristics

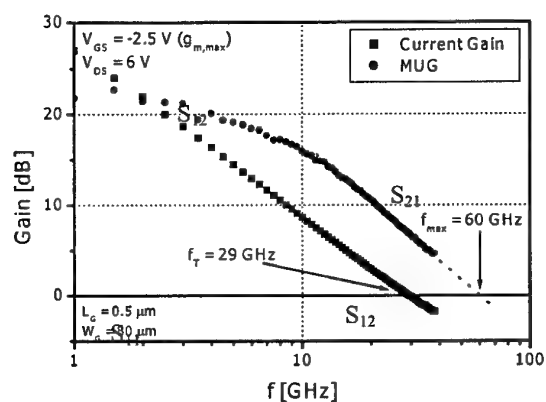


Figure 4: Maximum unilateral gain and current gain. The current gain cut off frequency  $f_T$  and the maximum frequency of oscillation  $f_{\text{max}}$  are indicated.

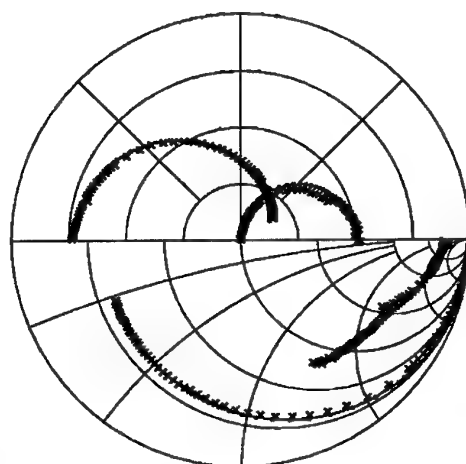


Figure 5: Hybrid chart indicating good agreement for S-parameters obtained from small signal model extraction as compared with measured data from a HEMT device ( $V_{\text{GS}} = -2.5\text{V}$ ,  $V_{\text{DS}} = 12\text{V}$ ,  $f = 50\text{ MHz} \dots 50\text{ GHz}$ ).

# First results of GaN MESFETs realized on (111) Si

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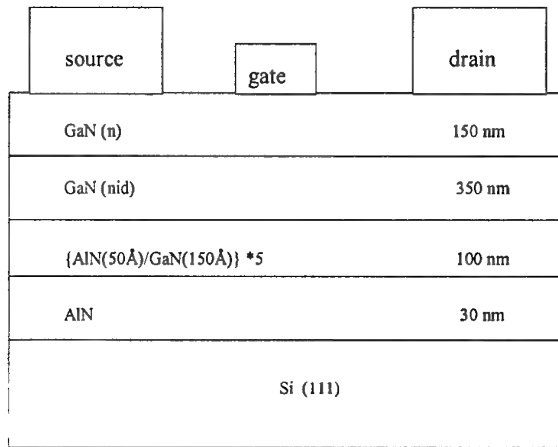
**Introduction :** In the high-power range, AlGaIn/GaN High Electron Mobility Transistors (HEMTs) on sapphire and on silicon carbide substrates exhibited high power results. These devices present respectively 3 W/mm at 18 GHz [1] and 9.8 W/mm at 10 GHz [2]. A power density of 2.2 W/mm with an associated power-added efficiency of 27% have been obtained on GaN MESFETs on sapphire substrate realized in our laboratory [3]. Today, we are also investigating GaN MESFETs on silicon substrate. A such substrate is very interesting for future trends [4]. Using materials wide band gap properties, we can also benefit of a low cost, advanced and mature technology on silicon substrate. In this communication, the process and the static results of the first GaN MESFETs realized on (111) Si substrates are presented. The epilayer growth was carried out at CRHEA and GaN MESFETs realization at IEMN.

**Device processing and static results :** The device structure was grown by low-pressure metal-organic vapor-phase epitaxy on a (111) silicon substrate in an AIXTRON AIX 200 reactor. A schematic cross section of this device structure is shown in Fig. 1. The process used for the realization of GaN MESFETs on silicon is the same as the process used for the realization of MESFETs on sapphire [3]. Devices with different source drain spacing from 2.5 to 4  $\mu\text{m}$  and different gate lengths from 0.5 to 2  $\mu\text{m}$  were fabricated. The gate is centered and the gate source spacing is 1  $\mu\text{m}$ . These devices are not passivated. The reverse breakdown voltage for a 2  $\mu\text{m}$  gate length and 4  $\mu\text{m}$  drain to source spacing is represented in Figure 2. This results in a breakdown voltage of about - 10 V for 1 mA/mm gate current density which is very suitable for power applications. Figure 3 shows a typical I-V curve for a 0.5  $\mu\text{m}$  gate length and a 2.5  $\mu\text{m}$  source-drain spacing MESFET. The gate bias ranges from - 8 to 1 V. The device demonstrates good pinch-off voltage characteristics. This allows to conclude in a good isolating buffer growth on silicon substrate. Moreover, the drain current density is higher than 100 mA/mm at  $V_{gs} = 1$  V and  $V_{ds} = 30$  V. This high drain to source voltage is also well appropriated for power applications. Finally, an extrinsic transconductance  $G_m$  greater than 30 mS/mm at  $V_{ds} = 20$  V can be observed in Figure 4. Moreover, the good pinch-off voltage is confirmed.

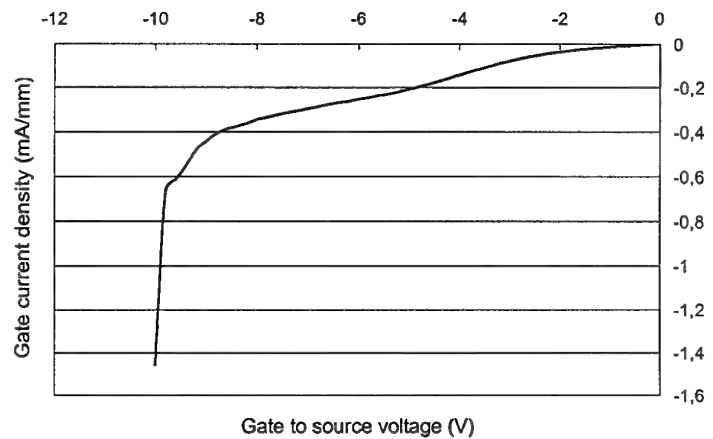
**Conclusion :** The first GaN MESFETs on (111) Si substrates have been realized using low-pressure metal-organic vapor-phase epitaxy. The devices demonstrate good pinch-off voltage characteristics and also support high voltage. This good holding voltage and the possibility to realize isolating buffer on silicon substrate make GaN MESFET on Si (111) very interesting for future wireless communication applications.

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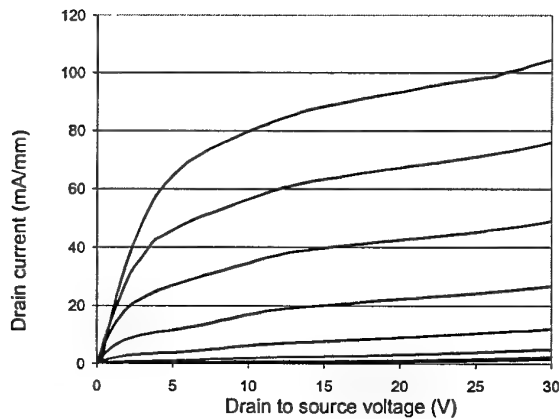
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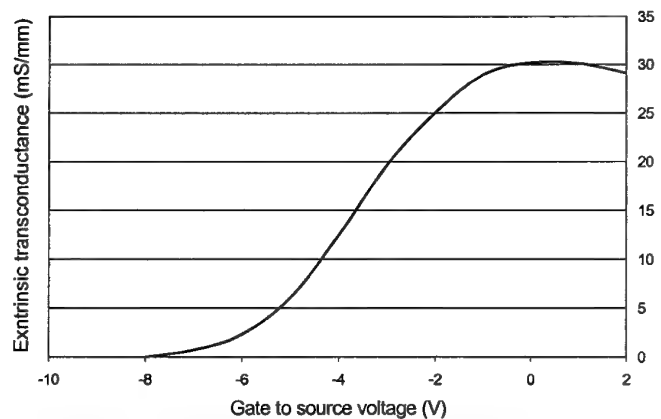
**Figure 1 :** Structure of the active layer and schematic device cross section



**Figure 2 :** Gate current density of a  $100 * 2 \mu\text{m}^2$  for  $V_{gs}$  from 0 V to -10 V



**Figure 3 :**  $I$ - $V$  characteristics of a  $100 * 0.5 \mu\text{m}^2$  for  $V_{gs}$  from -8 V to 0 V (step 1 V)



**Figure 4 :** Extrinsic transconductance for a  $100 * 0.5 \mu\text{m}^2$  for  $V_{gs}$  from -8 V to 2 V and  $V_{ds} = 20$  V

# Bias-dependence of AlGaN/GaN-HEMT small-signal equivalent circuit elements

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Bias-dependent broad-band S-parameter measurements (up to 40 GHz) followed by small-signal equivalent circuit parameter extraction according to ref. [1] have been performed on nitride-based HEMTs, which are of strong interest presently (see, e.g., [2]). As reported elsewhere [3], the intrinsic parameters were de-embedded from parasitic pad-capacitances, source and drain inductances as well as source and drain resistances,  $R_s$  and  $R_d$ . Here, we report on the bias-dependence of gate to source and gate to drain capacitances,  $C_{gs}$  and  $C_{gd}$ , transconductance,  $g_m$ , and drain to source resistance,  $R_{ds}$ , and their influence on the bias-dependent transit frequency,  $f_t$ . The role of the above mentioned parasitic  $R_s+R_d$ , including ohmic contact resistances which are a challenge in nitride technology currently [4], is discussed in detail. For this purpose, we have chosen a transistor with comparatively high  $R_s+R_d=5.3 \Omega\text{mm}$  having a maximum intrinsic  $f_t=3.7 \text{ GHz}$ . The sample under investigation was grown by MOVPE and consists of the usual GaN buffer followed by a 30 nm thick  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$  barrier layer. The gate width and length were 80 and 2  $\mu\text{m}$ , respectively.

Starting with a corroboration that the usual small-signal equivalent circuit model described in [1] is applicable for nitride-based HEMTs, we show in Fig. 1 the reconstruction of the DC output characteristics at different gate to source voltages,  $V_{gs}$ . The reconstruction has been done by integrating step by step extracted values of  $g_m$  or  $g_{ds} (=1/R_{ds})$  over  $V_{gs}$  or drain to source voltages,  $V_{ds}$ , respectively. We note that the extracted values of  $g_m$  and  $g_{ds}$  turn out to be positive, and, hence, cannot reconstruct a self-heating related decrease of the drain to source current,  $I_{ds}$ , at high  $V_{ds}$  and  $V_{gs}$ . Moreover, errors of integration accumulate successively. Nevertheless, both measurement and reconstruction are in acceptable agreement providing reliability of the data discussed later on.

Figs. 2 and 3 depict various parameters versus  $V_{ds}$  at  $V_{gs}=-1 \text{ V}$ . As expected,  $C_{gd}$  decreases with increasing  $V_{ds}$  while  $C_{gs}$  increases till they reach saturation. Obviously, the decrease of  $C_{gd}$  is more pronounced than the increase of  $C_{gs}$ , from which follows that the sum  $C_{gs}+C_{gd}$  is not independent of  $V_{ds}$ . Simultaneously,  $g_m$  and  $R_{ds}$  increase. Both de-embedded and extrinsic  $f_t$  (not shown) comply with the behavior of  $g_m$ , but the relative difference is a strongly decreasing function of  $V_{ds}$  (Fig. 3). According to ref. [5], this is due to (i) a resistive divider effect reducing the gain by the factor  $1+(R_s+R_d)/R_{ds}$  (see Fig. 4, circles) and (ii) the Miller effect increasing  $C_{gd}$  by the factor  $1+g_m(R_s+R_d)/(1+(R_s+R_d)/R_{ds})$  (see also Fig. 4, squares). Therefore, at low  $V_{ds}$ , the ratio  $(R_s+R_d)/R_{ds}$  affects the resulting

$$f_t = g_m / \{ 2\pi \{ [C_{gs}+C_{gd}][1+(R_s+R_d)/R_{ds}] + C_{gd}g_m(R_s+R_d) \} \},$$

provided the parasitic resistances are large relative to  $R_{ds}$  in this voltage region, as in the present case.

To conclude, bias-dependent parameter extraction based on small-signal equivalent circuit analyses has proven to be a powerful tool within III-nitride transistor characterization.

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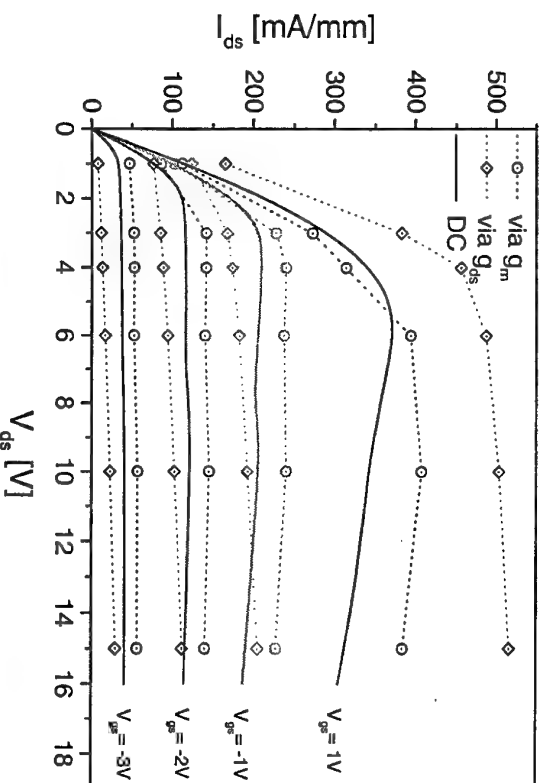


Figure 1: Comparison of DC output characteristics with reconstruction deduced from small-signal equivalent circuit parameters (integration of  $g_m$  over  $V_{gs}$  and  $g_{ds}$  over  $V_{ds}$ ).

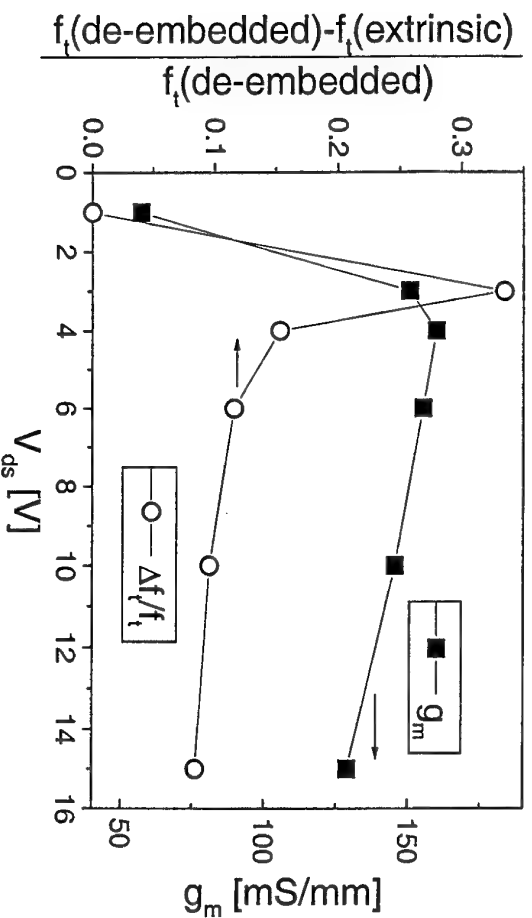


Figure 3: Transconductance and relative difference of de-embedded and extrinsic transit frequencies vs  $V_{ds}$ .  $V_{gs} = -1$  V.

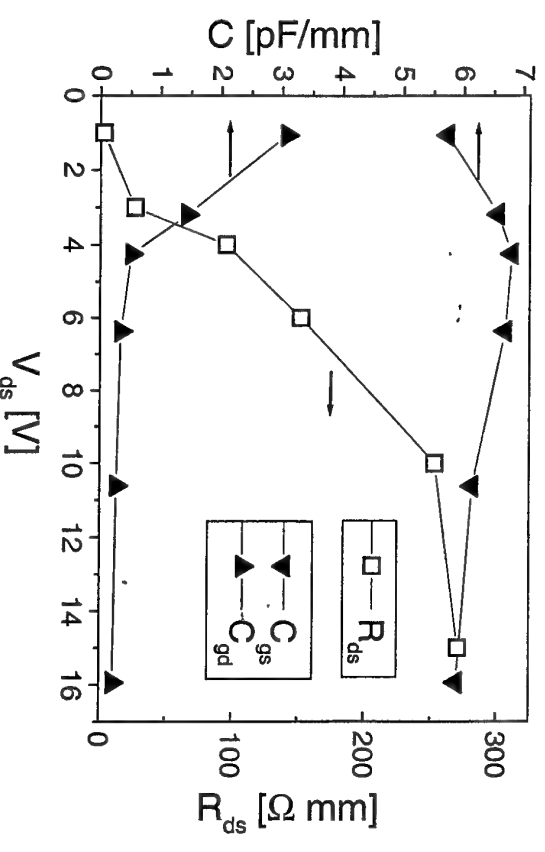


Figure 2: Bias-dependence of  $C_{gs}$ ,  $C_{gd}$  and  $R_{ds}$  at  $V_{gs} = -1$  V.

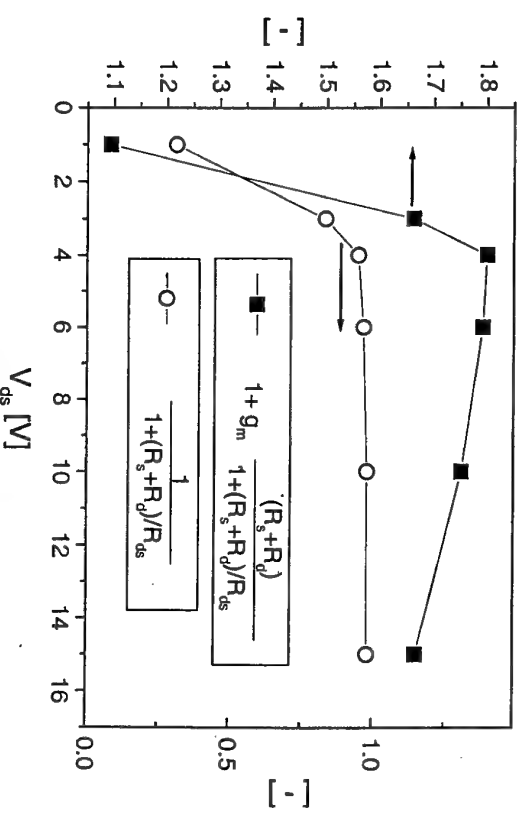


Figure 4: Important role of high parasitic resistances relative to  $R_{ds}$  at low  $V_{ds}$  on current gain (circles) a,  $C_{gd}$  (squares).  $V_{gs} = -1$  V.

# Characterisation of AlGaIn/GaN 2DEG structures by RoundHEMT application

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Transistors in the AlGaIn/GaN material system are predicted to deliver superior performance in high power applications at elevated temperatures. However, much work must be done to improve the quality of the epitaxial material. The high trap density e.g. results in a poorer high frequency performance than predicted from DC characteristics [1]. The effect of the traps can be observed by comparison of DC and pulsed I-V characteristics of GaN devices [2].

In this work we use the so called RoundHEMT designed for a very simple realisation of HEMT devices for DC, pulse and optoelectronic measurements. The RoundHEMT technology [3] satisfies the demands on a fast DC and moderate frequency transistor fabrication. It consists of a HEMT layout with the gate (G) formed as a closed ring, in contrast to the open finger in the conventional design. The drain (D) contact of the RoundHEMT is placed inside the gate ring, and the source metallisation (S) encloses the gate completely (Fig. 1). Only two metallization steps are needed for first investigations of epitaxial layers for HEMT purposes. This is a considerable simplification in comparison to the conventional HEMT, where a mesa etching is required.

The (opto-)electronic measurements are performed on an intentionally undoped AlGaIn/GaN layer system (3  $\mu\text{m}$  GaN, 20 nm  $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$  surface layer) grown by MOCVD on a sapphire substrate. The 2DEG data are  $N_{2\text{DEG}} = 5.6\text{E}12\text{cm}^{-2}$ ,  $\mu = 1180\text{ cm}^2/\text{Vs}$  at 300 K. Fig. 2 shows the DC output characteristics of a device. Optoelectronic measurements show a responsivity at wavelengths larger than the bandgap of GaN that clearly indicates the presence of deep traps in the layer system (Fig. 3). Pulse measurements ( $V_{\text{DS}} = \text{const}$ ,  $V_{\text{GS}} = \text{pulsed}$ ) show a very slow transient of the drain current (Fig. 4) that also indicates the existence of traps in the material.

As future work we will combine pulse measurements with optoelectronic measurements to investigate the spectrum of the trap levels.

In conclusion, the very simple RoundHEMT design allows the fast characterisation of important electronic and optoelectronic HEMT characteristics for a close feedback between epitaxy and device engineering.

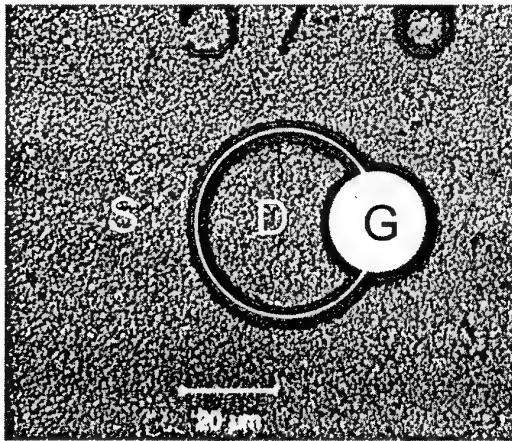


Fig. 1 SEM picture of a RoundHEMT  
Channel width: 100  $\mu\text{m}$   
Gate length: 700 nm

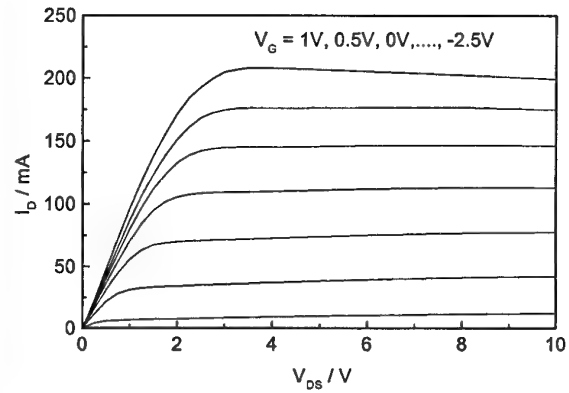


Fig. 2 Output characteristics

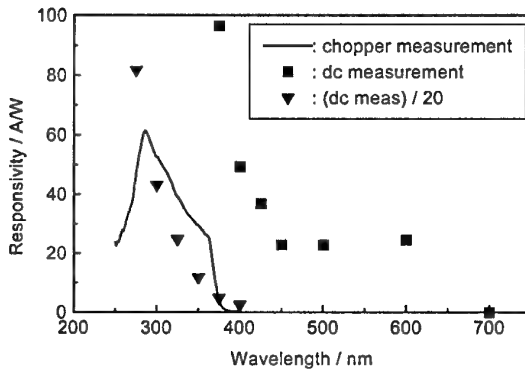


Fig. 3: Optoelectronic measurements  
chopper: measurement using lock-in technique with 130Hz chopping frequency  
dc: photocurrent after transient processes

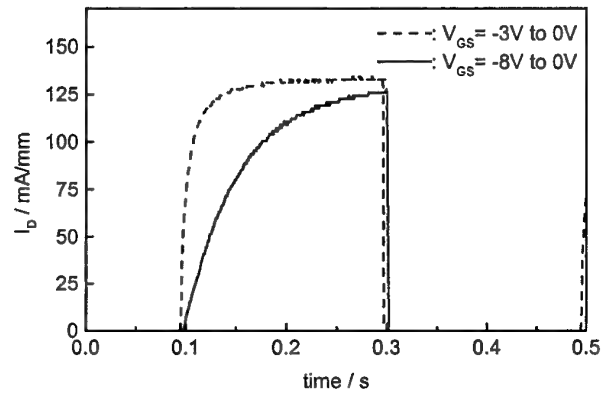


Fig. 4: Pulse measurements  
 $V_{DS} = 10\text{V}$   
 $V_{GS}$ : pulsed with 400ms periode

#### References:

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## MULTIWAFAER 6 INCH MOVPE PLANETARY REACTOR® FOR ELECTRONIC DEVICE PRODUCTION

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The increasing demand for high performance, low cost GaAs and InP based devices pushes the MOVPE growth technology towards larger wafer sizes. To meet the industrial requirements we developed the Planetary Reactor® concept with the capability to grow on five 6 inch wafers simultaneously (see Fig. 1). We optimized the thickness uniformity of GaAs, InGaP, and AlInGaP layers by varying the carrier gas total flow from 17 sl/min to 34 sl/min. By this the radial position of the maximum of the growth rate can be neatly tuned inwards and outwards across the susceptor radius. The optimum thickness uniformity of  $\pm 0.5\%$  was obtained for a carrier gas flow rate of 24 sl/min (see Fig. 2, right scale). The efficiency of the group III precursors was found to vary with the carrier gas flow rate from 40% up to 54% with the highest values obtained at the low end of the carrier gas flow rate range (see Fig. 2, left scale). GaInP layers grown under these optimized conditions showed wavelength homogeneities of 0.9% with a mean peak wavelength of 652.3 nm measured on a 6" wafer. Six inch AlGaAs/GaInP/AlGaAs test structures exhibited wavelength homogeneities as good as 0.2% with a mean peak wavelength of 689.7 nm. Under optimized conditions undoped GaAs layers with background electron concentrations and mobilities of  $n_{77\text{ K}} = 4 \times 10^{13} \text{ cm}^{-3}$ ,  $\mu_{77\text{ K}} = 100,000 \text{ cm}^2/\text{Vs}$  and  $n_{300\text{ K}} = 6 \times 10^{13} \text{ cm}^{-3}$ ,  $\mu_{300\text{ K}} = 8000 \text{ cm}^2/\text{Vs}$  at 77 K and room temperature, respectively, were routinely achieved. At a free electron concentration of  $n = 1.1 \cdot 10^{18} \text{ cm}^{-3}$  mobilities of  $\mu = 1600 \text{ cm}^2/\text{Vs}$  were achieved in doped layers. The standard deviation of the sheet resistance across a 6 inch wafer was as low as 2.7%.

To investigate the dependence of the growth rate on the position along the susceptor radius AlAs/GaAs distributed Bragg reflectors (DBR) were grown with one 6 inch dish intentionally stopped. High resolution X-ray spectra were recorded across the diameter of the 6 inch wafers. Fig. 3 shows the XRD profile along the diameter of the stopped wafer. The decrease of the satellite spacing indicates a gradient in layer thickness, hence growth rate, from the center to the rim of the susceptor. This gradient can be utilized to tune the thickness uniformity by rotating the dishes through the depletion gradient. Fig. 4 shows the XRD profile of a rotated 6 inch wafer from the same run. The fringes are equidistant across the wafer diameter indicating an excellent thickness uniformity of the layers. The wafer appeared green to the unaided eye without any visible color changes and inhomogeneities. Reflectance measurements showed an average reflected wavelength of 552.4 nm with an overall standard deviation of 3.1 nm corresponding to 0.5%.

Additional data on doping, photoluminescence and structural properties will be presented. The dependence of wavelength, intensity and conductivity homogeneity on the process parameters will be discussed.

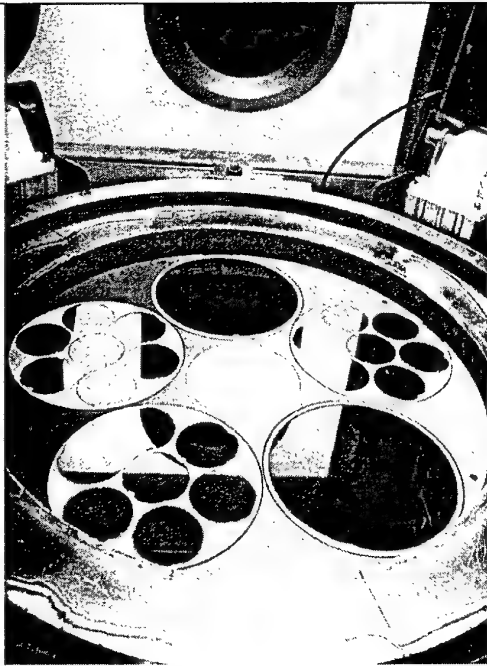


Fig. 1: AIX 2600 G3 system in the 5x6 inch configuration. The 2 inch wafers are shown for reference.

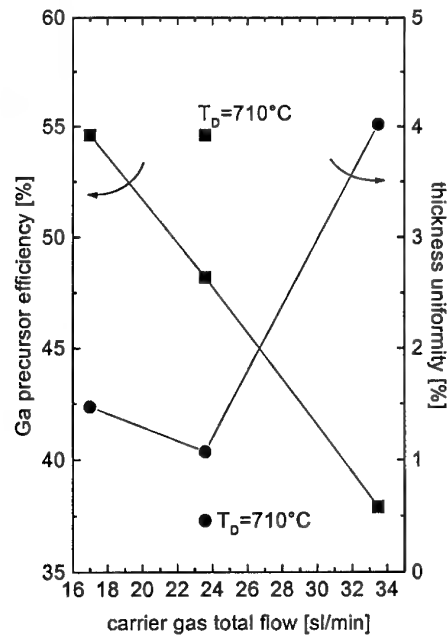


Fig. 2: Gas precursor efficiency and thickness uniformity as a function of carrier gas total flow.

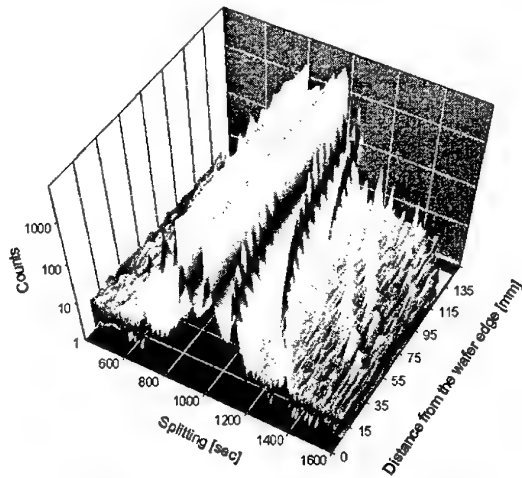


Fig. 3: High resolution XRD measurements of a 6 inch stopped wafer as a function of position on the wafer.

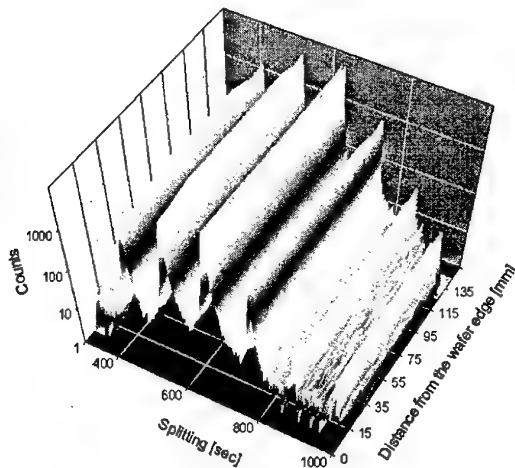


Fig. 4: High resolution XRD measurements of a 6 inch rotated wafer as a function of position on the wafer.

# Deep traps related effects in GaN MESFETs grown on sapphire substrate

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The wide bandgap semiconductor gallium nitride (GaN) and related materials are highly attractive for high-power and high-temperature applications [1]. However, instabilities related to material and trapping effects limited the reproducibility and the performance of these devices. A decrease of the drain current,  $I_D$ , during operation and after repeated measurements has been observed by several authors [2,3], and generically identified as "current collapse".

In this work we have investigated the mechanisms that lead to  $I_D$  decrease in GaN MESFETs grown by MOCVD on a (0001) sapphire substrate, see Fig. 1, in the attempt to identifying the deep traps involved. Results can be summarized as follows:

(i) When these devices are biased at high  $V_{DS}$  or simply by repeating measurements in the dark, a large degradation occurs, consisting in a decrease of drain current with respect to the untrapped condition, realized by shining sub-bandgap light on the device, see Fig. 2. By measuring the  $I_D$  vs  $V_{GS}$  characteristics in the linear region before and after high  $V_{DS}$  bias keeping the device in the dark, we can observe, see Fig. 3 that the  $I_D$  degradation is due to a remarkable positive threshold voltage shift  $\Delta V_{th}$  and a slight decrease in transconductance  $g_m$ . A complete recovery of both  $V_{th}$  and  $g_m$  takes place after a subsequent illumination of the device (Fig. 3). The  $V_{th}$  shift implies that trapping occurs under the gate, while the decrease in transconductance is possibly related to an increase in drain series resistance.

(ii) Devices showing current decrease after biasing in saturation at  $V_{DS} = 20$  V were submitted to phototransient experiments, see Fig. 4. When the light is turned on, a remarkable increase in drain current is observed, consequent to electron detrapping. After turning off the light,  $I_D$  slowly returns to the "collapsed" value, with capture times which are thermally activated with  $E_C \simeq 0.1$  eV. This process is similar to the persistent photoconductivity effect already observed in GaN bulk material [4,5]. We have also observed that the capture time decreases at increasing the electric field in the gate-drain region, i.e. by decreasing  $V_{GD}$ , but is rather insensitive to  $V_{GS}$ , not shown, thus suggesting that the traps responsible for the collapse are under the gate and in the gate-drain access region. This also points out a difference between trapping experiments in bulk material and in real devices: in the latter case, the presence of high electric fields reduces remarkably the capture times, thus leading to a faster current decay time ( $\sim$  minutes) with respect to those observed in GaN bulk material ( $\sim$  hour) [4,5].

(iii) The effects of the capture time on device characteristics can be seen in Figs. 5,6. When illuminated by a sub-bandgap white light, devices present the maximum drain current, see Fig. 5; in DC conditions, two repeated measurements in the dark with  $V_{DS} > 10$  V are sufficient to reach a strong collapsed condition (curve (3) in Fig. 5). Some trapping occurs even under illumination, see inset of Fig. 5, but can be reduced if measurements are carried out using short pulses, using either HP4142 (1ms) or a Transmission Line Pulse system (560ns). Unlike during DC measurements, repeated PULSE (1ms) and TLP (560ns) measurements in the dark cause a slighter  $I_D$  degradation, Fig. 6, pointing out the importance of the measurement technique and of the device conditions on the  $I-V$  characteristics that can be obtained.

(iv) Following the method described in [6], by measuring the current increase  $\Delta I(h\nu)$  induced by light with respect to the fully collapsed dark value  $I_{dark}$ , as a function of the photon energy, four transition energies have been identified at 1.75 eV, 2.32 eV, 2.67 eV, and possibly at 3.15 eV, see Fig. 7. The values at 1.75 eV and 2.67 eV are well correlated with measurements reported in [6] and with persistent photoconductivity or photocapacitance measurements [8,9,10]. Finally, the behavior of the drain current measured in the dark depends not only on the equilibrium between electron capture and emission processes: in fact, non-negligible hot-carrier-induced radiation electroluminescence is observed in the visible and UV region, see Fig. 8. The emitted radiation can contribute to detrapping electrons even during measurements in the dark, thus causing a slight increase in  $I_D$  at high  $V_{DS}$ , as can be seen from the dark output  $I-V$  (Fig. 2).

In conclusion, a detailed analysis of trapping phenomena in GaN MESFETs has been reported, which provides tools for a more precise characterization and localization of deep traps levels and points out the importance of the bias and device conditions on the measured electrical characteristics.

**Acknowledgments:** This work was partially supported by the ASI Project, MURST and Progetto Finalizzato CNR MADESS II.

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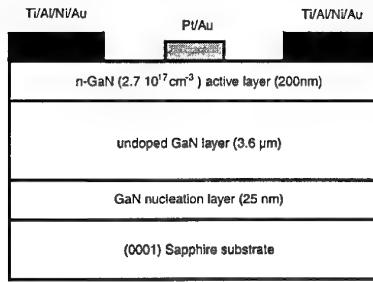


Fig.1: Schematic cross-section of the tested GaN MESFETs. Devices have a source-drain spacing of  $2.3\mu\text{m}$ , a gate length of  $0.3\mu\text{m}$  and a gate-drain spacing of  $1\mu\text{m}$ . Gate width is  $2 \times 50\mu\text{m}$ .

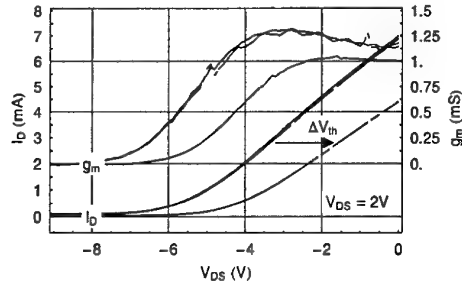


Fig.3:  $I_D$  vs  $V_{GS}$  measurements at  $V_{DS} = 2\text{V}$ . Continuous line: unstressed device; dashed line: after 20 minutes at  $V_{GS} = 0\text{V}$ ,  $V_{DS} = 20\text{V}$ ; dotted line: recovery after 30s of sub-bandgap white light illumination.

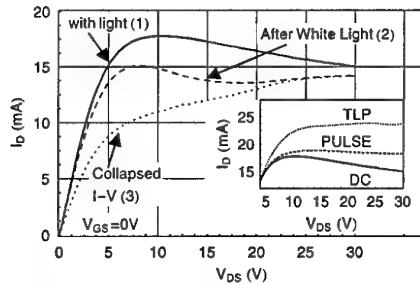


Fig.5: Repeated DC output I-V characteristics at  $V_{GS} = 0\text{V}$ . The first measurement (1) was carried out with a sub-bandgap white light. Then, in the dark, the subsequent measurement (2) induces the charge trapping, giving rise to an I-V collapse (3) (third measurement). Inset: I-V characteristics with sub-bandgap white light at  $V_{GS} = 0\text{V}$ . In DC conditions, trapping phenomena and self heating cause a decrease of  $I_D$  even under illumination. Both are reduced by using  $1\text{ms}$  pulses (PULSE). By adopting short (560ns) TLP pulses, trapping effects are virtually eliminated.

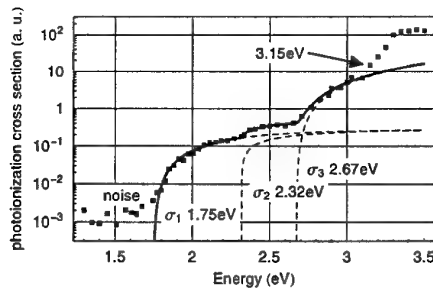


Fig.7: Spectral dependence of the photoionization cross section  $\sigma$ . The closed symbols are the experimental data, while the solid line is the fitting obtained. For energies lower than  $1.7\text{eV}$  no significant data has been obtained (noise). The dashed lines represent the three fitted photoionization cross section using the analytical forms reported in [7], i.e. (i)  $\sigma_1 = 4.8(h\nu - 1.75)^{3/2}/(h\nu)^3$ , (ii)  $\sigma_2 = 0.86(h\nu - 2.32)^{1/2}/(h\nu)$ , (iii)  $\sigma_3 = 72(h\nu - 2.67)^{3/2}/(h\nu)$ .

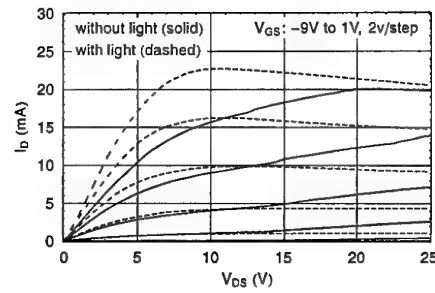


Fig.2: Collapse of the I-V characteristics observed after some measurements up to  $V_{DS} = 25\text{V}$  (continuous lines). The characteristics of an untreated device illuminated by sub-bandgap white light are also shown for comparison (dashed lines).

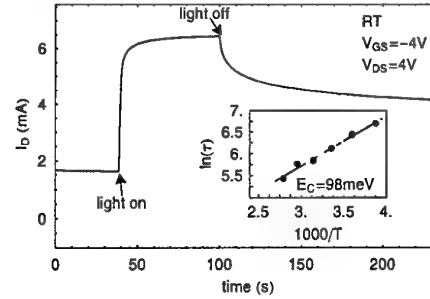


Fig.4: Typical behaviour of the measured  $I_D$  for the dark to light (emission) and light to dark (capture) conditions. In the inset the Arrhenius plot of the capture time constant  $\tau$  is depicted, from which a capture energy barrier  $E_C = 98\text{meV}$  has been extracted.

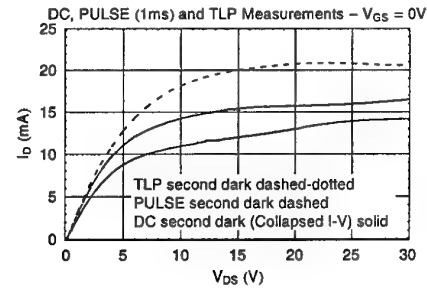


Fig.6: Second measurements carried out in the dark starting without trapped charge. The bias time dependent charge trapping is reduced going from DC measurements (continuous line), to pulsed ( $1\text{ms}$ ) (dashed line) and to TLP ( $560\text{ns}$ ) (dashed dotted line).

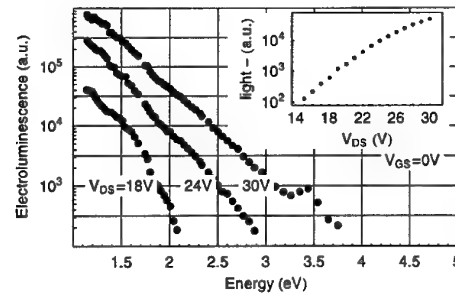


Fig.8: Electroluminescence spectra carried out on a typical device at  $V_{GS} = 0\text{V}$ . The inset reports light intensity (integrated in the  $1.6\text{eV} - 6\text{eV}$  range) vs  $V_{DS}$  at  $V_{GS} = 0\text{V}$ . Non negligible light emission take place for  $V_{DS} > 15\text{V}$ .

# Ohmic contacts studies on AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs

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Low resistance ohmic contacts are required in the successful implementation of High Electron Mobility Transistors (HEMTs). A few attempts to achieve good ohmic contacts on AlGa<sub>N</sub> or Ga<sub>N</sub> epilayers have been reported in the literature and are summarized in the table:

References	Metallization	Thickness Å	RTA conditions	Contact resistance Ω.mm	Specific contact resistivity Ω.cm <sup>2</sup>	Nature of the cap layer
[1] n°1	Ti/Al/Pt/Au	200/800/400/1500	900°C, 35 s	0.039	5.38x10 <sup>-8</sup>	Al <sub>0.15</sub> Ga <sub>0.85</sub> N
[2]/[3] n°2	Ti/Al/Ti/Au	100/500/250/300	850°C, 60 s	0.75	*	GaN
	Ti/Al/Ti/Au/WSiN	100/500/250/300/1200	850°C, 60s	0.62	*	GaN
[4] n°3	Ti/Al/Ni/Au	150/2200/400/500	900°C, 30 s	*	8.9x10 <sup>-8</sup>	GaN
[5]	Ti/Al	200/1000	900°C, 30 s	*	8x10 <sup>-6</sup>	GaN

In our laboratory, we have shown that after an annealing performed at 900°C for 30 s, the specific contact resistivity of Ti/Al/Ni/Au contact on Ga<sub>N</sub> layer was lower than Ti/Al contact on Ga<sub>N</sub> layer [6]. Moreover, Ti/Al/Ni/Au contacts had the best morphology and were stable at up 600°C for 5 days.

To improve the contact resistance, we decided to compare three different composite metal layers (n°1, n°2, n°3) on the same epitaxial structure which is described in figure 1.

Just before the metal deposition, the AlGa<sub>N</sub>/Ga<sub>N</sub> samples were dipped in a concentrate HCl solution during 3 min, blown dry with nitrogen and followed by an in situ Ar<sup>+</sup> plasma etching to deoxidize the surface. These three contact metal systems were deposited by electron beam evaporation. The same rapid thermal annealing (RTA) was performed at 900°C for 40 s in N<sub>2</sub> atmosphere to realize the ohmic contacts for all the samples. The mesa etching was performed by reactive ion etching using SiCl<sub>4</sub>.

Current-Voltage (I-V) characteristics and atomic force micrographs (AFM) of these different annealed metal contacts are presented in figure 2. We can observe that the low resistance ohmic contact and the best morphology are obtained with Ti/Al/Ni/Au contact.

We also have investigated the evolution of specific contact resistance according to annealing temperatures and times for AlGa<sub>N</sub> layer with 15 % and 30 % of Al content for Ti/Al/Ni/Au contact.

Figure 3 shows the evolution of the ohmic contact resistivity versus the annealing temperatures and times. We achieved the best results for an AlGa<sub>N</sub> layer (30% of Al content) doped with Si to 1x10<sup>18</sup> cm<sup>-3</sup> using Ti/Al/Ni/Au contact annealed at 900°C during 50 s in N<sub>2</sub> atmosphere (figure 3). The contact resistance was as low as 0.46 Ω.mm with a specific contact resistivity of 9.3x10<sup>-6</sup> Ω.cm<sup>2</sup>.

Figure 4 shows the evolution of the root mean square (RMS) surface roughness versus the annealing temperatures and times. We observe that the surface roughness is in the order of 400Å.

We will also show the stability of specific contact resistance with subsequent aging treatments.

In summary, we have tested three different composite systems for ohmic contacts on AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs and we have demonstrated that the best composite metal layer is Ti/Al/Ni/Au in our case, as we previously demonstrated on Ga<sub>N</sub> [6].

## Acknowledgments

This work was carried out with the financial help of the DGA (French Army), Contract N°97-065.

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AlGaIn 300Å $X_{Al} = 10\%$
GaN nid 3µm
Sapphire substrate

Figure 1 : layer structure.

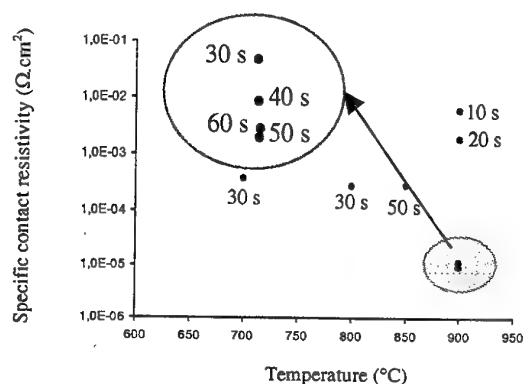


Figure 3 : Evolution of the specific contact resistivity according to annealing temperatures and times for AlGaIn layer with 30 % of Al content for Ti/Al/Ni/Au contact.

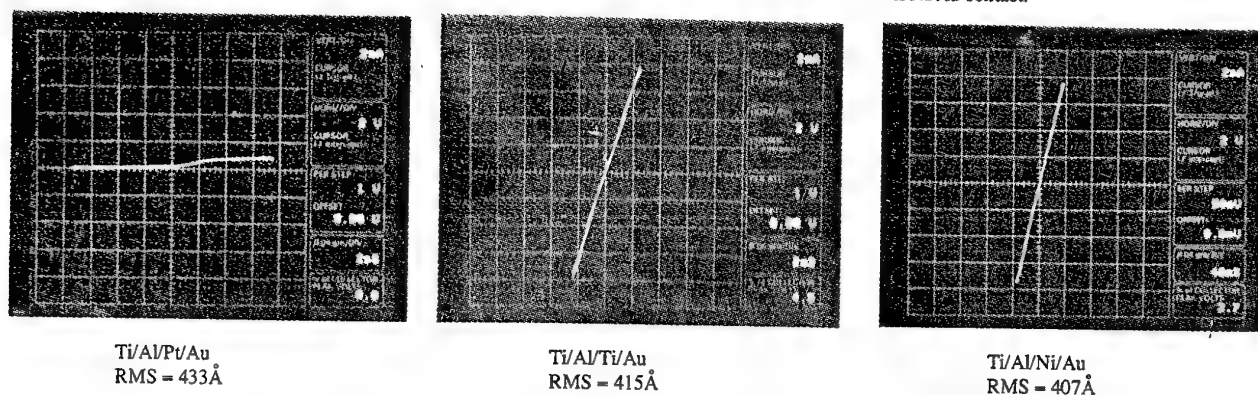


Figure 2 : I(V) characteristics of the ohmic contacts after annealing at 900°C during 40 s.

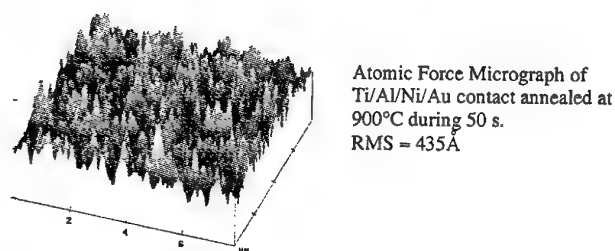


Figure 4: Evolution of roughness according to annealing temperatures and times for AlGaIn layer 30 % of Al content for Ti/Al/Ni/Au contact.

## Mesa etching and gate recessing of n-type GaN: photoelectrochemical approach

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It is well known that III-nitrides are chemically inert materials and thus resistant to room-temperature wet etching. Therefore dry etching techniques like RIE or CAIBE are commonly applied to etch III-nitrides. But for device processing, mainly for gate recessing, a low-damage etching technique is a necessity. Mesa etching, in addition, requires sufficiently high etch rates generally a problem for dry etching techniques. Recently, photoenhanced wet chemical etching of GaN has been reported [1], but little is known about gate recess etching [2]. On the other hand, discrepancies concerning the etch conditions (solution composition, light intensity) and surface properties (smooth etching, whiskers formation, etc.) can be found in published results.

In our contribution, a comprehensive study of photoenhanced wet etching of GaN for gate recessing as well as for mesa etching is presented. AZ400K solution was used as an etchant and test structures were analyzed by means of the SEM. The main results are as follows:

- The etching process is strongly dependent on the structural quality of the used GaN layers, as well as on the composition of the KOH-based solution and the light intensity.
- The etched surface exhibits a higher roughness than the original GaN surface.
- Whiskers are observed when deeper etching (>150 nm) is performed.
- The etch rate at the etching conditions convenient for gate recessing is about 20 nm/min.
- Trenches in the vicinity of the etch mask are observed at low intensity illumination and higher concentration of the etchant.
- Etching conditions tested for mesa etching gave an etch rate of about 160 nm/min.

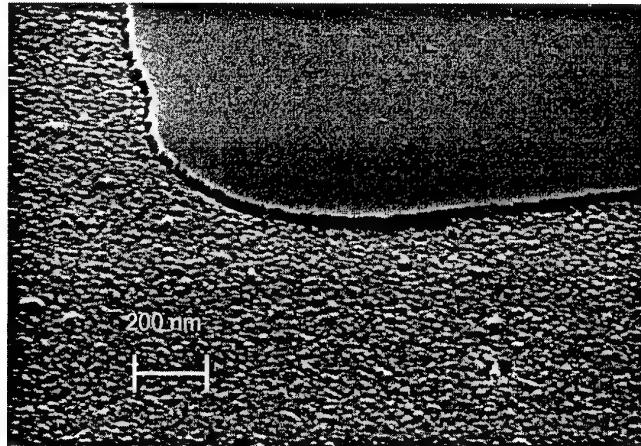
The obtained knowledge can be used for more controllable application of the photoelectrochemical etching of GaN. Resulting mesa etched structures exhibited satisfactory electrical isolation and the etched surface intended for gate recessing has a roughness of about 4.5 nm RMS measured by AFM.

### References:

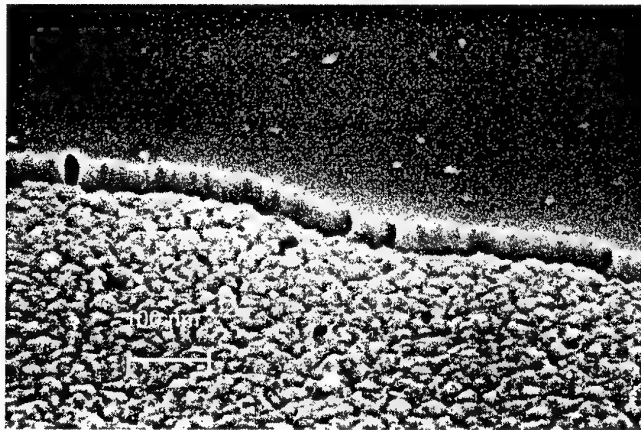
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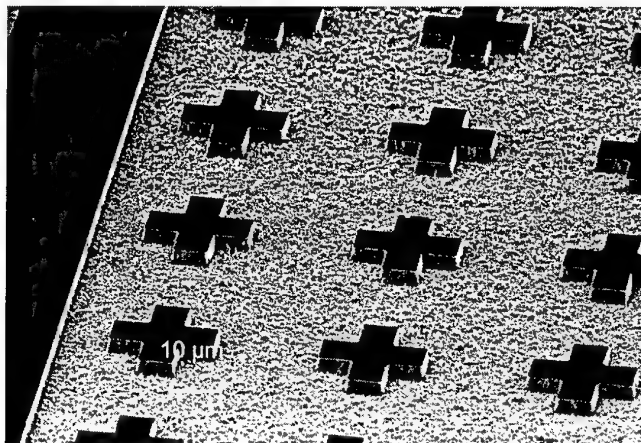
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**Figure 1:** SEM micrograph of n-GaN layer ( $n \sim 2.5 \times 10^{18} \text{ cm}^{-3}$ ) etched for 100 seconds. The etch depth is about 33 nm.



**Figure 2:** SEM micrograph of n-GaN layer ( $n \sim 2.5 \times 10^{18} \text{ cm}^{-3}$ ) etched for 150 seconds. The etch depth is about 55 nm.



**Figure 3:** SEM micrograph of mesa etched n-GaN layer ( $n \sim 2.5 \times 10^{18} \text{ cm}^{-3}$ ). The etching was performed down to the substrate

## **SESSION F**

### **III V Devices**

# Design and realization of sub 100nm gate length HEMTs

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Improvement in e-beam lithography allows us to reduce the gate length of HEMTs at some tens of nanometers. Using such small gate lengths it will be possible to obtain HEMTs with  $f_t$  greater than 300 GHz and  $f_{max}$  greater than 500 GHz using the InAlAs/InGaAs/InP material system. The realisation of these high performance devices will allow the development of several new applications like passive radiometry and ultra high bit rate transmission links.

In order to reach this goal, the design of the layer and device technological parameters represents a key point. We first present the simulation work performed to optimise the structural parameters of a 50nm gate device.

For improving the performance of devices, the reduction of the gate length is obviously the main point but this is not sufficient to obtain state of the art results. The aspect ratio defined as the gate length over the gate to channel distance has to be kept high enough to avoid short channel effects [1]. First, we used a classical simulator, the software Helena, to optimise the active layer structure and the charge control. Second, a 2D Monte Carlo model was used to accurately simulate sub 100nm gate device [2]. With this tool, the doping level in the  $\delta$ -doped layer and the length of the recess were optimised. The 50 nm gate length optimised device topology is presented in Fig1. The device process is in progress.

65nm gate HEMTs were already realised on a non optimised layer. First, the mesa was defined by  $H_3PO_4:H_2O_2:H_2O$  solution (5:1:40). For the ohmic contacts, Ge/Au/Ni/Au was evaporated followed by 1 min RTA at 300 °C. Typical ohmic contact resistance of 0.15 to 0.2  $\Omega$ .mm was measured by TLM method. The T-shaped gate was defined using a trilayer resist technique. In order to remove InGaAs cap layer, selective Succinic Acid (SA): $NH_4OH:H_2O_2$  solutions was used. Finally Ti/Pt/Au gate was evaporated as well as the bonding pads. We obtained a maximum cutoff frequency  $f_t$  of 270 GHz (fig. 2), which is a result close to the state of the art for this gate size.. The small-signal equivalent circuit of this transistor at  $V_{ds} = 0.8V$  and  $I_d = 260mA/mm$ , is shown in Fig. 3.

However, the extrapolated maximum frequency of oscillation  $f_{max}$  is only 250 GHz. This last point shows the necessity to use an 'optimised' layer structure for the 50 nm length gate, to improve the ratio  $G_m/G_d$  and  $C_{gs}/C_{gd}$  and  $f_{max}$  consequently.

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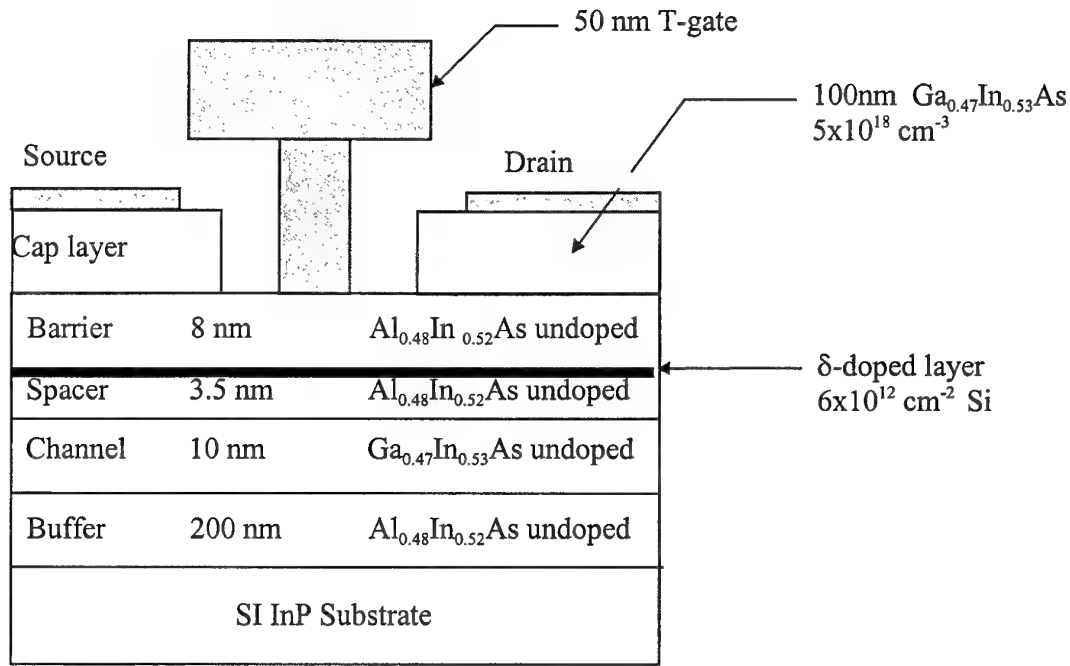


Figure 1 : New layer structure optimised for 50nm gate.

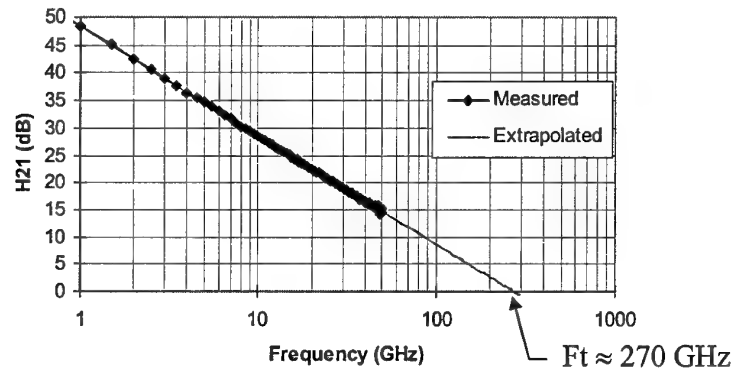


Figure 2 : Maximum current gain obtained for a 65nm x 100  $\mu\text{m}$  InP HEMT at the polarisation  $V_{ds}=0.8\text{V}$  and  $I_d=260 \text{ mA/mm}$ .

Element	$G_m$	$G_d$	$C_{gs}$	$C_{gd}$	$C_{ds}$	$R_i$	$R_g$	$R_s$
Value	120 mS	16 mS	45.1 fF	8.1 fF	6.4 fF	4.2 $\Omega$	5.8 $\Omega$	3.7 $\Omega$
Element	$R_d$	$L_g$	$L_s$	$L_d$	$C_{pg}$	$C_{pd}$	$\tau$	
Value	4.9 $\Omega$	30 pH	1 pH	30pH	1 fF	22 fF	-0.2 ps	

Figure 3 : Small-signal equivalent circuit model of 65nm x 100  $\mu\text{m}$  InP HEMT at  $V_{ds} = 0.8\text{V}$ ,  $I_d = 260 \text{ mA/mm}$ .

The results shown on the fig. 2 and 3 are found with a HEMT processed on a 'classical' layer structure, designed for 0.1  $\mu\text{m}$  gate.

# Topology's influence on gate ionisation currents of a quasi Enhancement-mode $\text{Al}_{0.67}\text{In}_{0.33}\text{As}/\text{Ga}_{0.66}\text{In}_{0.34}\text{As}$ metamorphic HEMT.

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This paper presents original results provided by combination of Enhancement-Mode (E-mode) with metamorphic growth of  $\text{Al}_{0.67}\text{In}_{0.33}\text{As}/\text{Ga}_{0.66}\text{In}_{0.34}\text{As}$  HEMT structure on a GaAs substrate. The devices exhibit good dc and rf performance. Excellent Schottky characteristics have been obtained (a typical reverse gate to drain breakdown voltage of  $-16\text{V}$ ). The  $0.4\mu\text{m}$  gate length devices have a saturation current of  $400\text{mA/mm}$  at  $+0.8\text{V}$  gate voltage. Gate current studies, versus gate-to-drain extensions and cap layer thickness have been studied, for the first time, in these devices, showing the gate current issued from impact ionization. The only work reported, to our knowledge, using a metamorphic HEMT structure in Enhancement-mode with an indium content close to 50% have been made by K. Eisenbeiser & al.[1]. Their typical gate-to-drain breakdown voltage was  $-5.2\text{V}$ , a current density of  $220\text{mA/mm}$  at  $V_{\text{gs}}=+0.6\text{V}$  and an extrinsic transconductance of  $650\text{mS/mm}$ . The  $0.6\mu\text{m}\times 3\text{mm}$  devices exhibited  $30\text{mW/mm}$  at  $850\text{MHz}$ .

The Enhancement mode device is interesting since it eliminates the need for a negative voltage supply on a chip. Recent works on E-mode  $\text{AlInAs}/\text{GaInAs}$  HEMT's on InP substrates have demonstrated superior microwave and low noise performance over Pseudomorphic HEMT's on GaAs substrates [2,3]. GaAs substrates are more suitable for large scale MMIC production contrary to InP substrates which are fragile, difficult to etch, not available in large scale and more expensive. A way to avoid InP substrate is to use metamorphic (MM) buffers to accommodate the lattice mismatch between the active layer and the GaAs substrate. We have used an inverse step-graded buffer of  $\text{AlInAs}$  [4,5,6] and we benefit of the indium composition close to 30% for power application. The high  $\Delta E_c$  of  $0.7\text{eV}$  leads to high sheet carrier density and good confinement [5]. The high bandgap of  $\text{InAlAs}$  and  $\text{InGaAs}$  as compared to higher indium content allows respectively a good Schottky barrier height that improves breakdown voltage and reduces the impact ionization.

The layers were grown on (100)-oriented GaAs substrate using a Riber 32P Molecular Beam Epitaxy machine. Figure 1 show the simple heterostructure. The fabrication started with the realization of source and drain ohmic contacts. For the ohmic contact formation,  $\text{Ge}/\text{Au}/\text{Ni}/\text{Au}$  metallisation and a rapid thermal annealing at  $340^\circ\text{C}$  during 60s under  $\text{N}_2/\text{H}_2$  is performed. TLM (Transmission Line Model) measurements show a typical ohmic contact resistance  $R_c$  of  $0.20\Omega/\text{mm}$ . Device isolation was performed by a non selective chemical mesa etching down to the  $\text{AlInAs}$  buffer layer with  $\text{H}_3\text{PO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$  (5:1:40) etchant. The T-gate was defined using a bilayer resist ( $\text{PMMA}/\text{P}(\text{MAA}-\text{MAA})$ ) to improve lift-off. After the chemical recess using a selective etchant (succinic acid/ $\text{H}_2\text{O}_2$ ), the gate metallisation is e-beam evaporated and consists of  $\text{Ti}/\text{Pt}/\text{Au}$  sequence. The etching selectivity ratio of  $\text{InGaAs}$  over  $\text{AlInAs}$  is greater than 500. A typical Schottky characterization gives an ideality factor  $\eta$  of 1.7 and a Schottky barrier height  $\Phi_b$  of  $1.275\text{eV}$  ( $V_{\text{bi}}=0.75\text{V}$ ). As the final step, thick  $\text{Ti}/\text{Au}$  contacts were deposited for microwave probing pads.

DC and microwave characteristics of  $100\mu\text{m}$  wide MM-HEMT's were measured on wafer. Hall effect measurements are used to determine the sheet carrier density  $n_H$  and electron mobility  $\mu_H$ . They are, respectively,  $3.9\times 10^{12}\text{cm}^{-2}$  and  $7000\text{cm}^2/\text{V.s}$  at room temperature ( $300\text{K}$ ).

The I-V characteristic is given in figure 2. We processed two structures: the thin cap layer ( $10\text{nm}$ ) and the thick cap layer ( $25\text{nm}$ ). Also, we processed devices with three source-to-drain extensions ( $L_{\text{SD}}=1.3\mu\text{m}$ ,  $1.8\mu\text{m}$  and  $3\mu\text{m}$ ). We fixed the gate at  $0.5\mu\text{m}$  from the source. Thin cap devices (resp. thick cap) exhibit a drain-to-source current  $I_{\text{DS}}=400\text{mA/mm}$  (resp.  $360\text{mA/mm}$ ) at a gate-to-source voltage  $V_{\text{GS}}=+0.8\text{V}$  and a typical extrinsic transconductance is  $490\text{mS/mm}$  (resp.  $510\text{mS/mm}$ ). S-parameter measurements were carried out and the current gain cut-off frequency  $f_T$  were estimated. An extrinsic current cut-off frequency  $f_{\text{r}}$  of  $62\text{GHz}$  and the cut-off frequency  $f_{\text{MAG}}$  of  $210\text{GHz}$  are achieved with the  $0.4\mu\text{m}$  gate length device. They have been obtained at maximum transconductance bias condition ( $V_{\text{DS}}=2\text{V}$  and  $V_{\text{GS}}=0.2\text{V}$ ). The Schottky characteristic curve for device with  $L_g=0.4\mu\text{m}$  is shown in figure 3. For thin cap devices (resp. thick cap), a maximum gate-to-drain voltage of  $-16\text{V}$  (resp.  $-14\text{V}$ ) at the gate current of  $500\mu\text{A/mm}$  were obtained. The good results in the Schottky diode are in a large part attributed to well controlled recess process. Figure 4 shows gate characteristic. For a same gate current issued from impact ionization (around  $0.1\mu\text{A}$ ), we have an applied drain voltage of  $4\text{V}$  (resp.  $3\text{V}$ ) for thin cap devices (resp. thick cap). Thin cap devices have a better breakdown voltage. For these devices, we obtain a constant source resistance of  $4.1\Omega$ . Equivalent circuit parameter extracted from measurements shows a  $C_{\text{GS}}$  of  $330\text{fF}$  independent of  $L_{\text{SD}}$  and a decrease of  $C_{\text{GD}}$  versus  $L_{\text{SD}}$  (from  $124$  to  $9\text{fF}$ ). The figure 5 shows the gate current characteristic for a large extension. At pinch-off ( $V_{\text{GS}}<V_{\text{p}}$ ), we see the current issued from tunneling effects. It is very small because we have a large diode breakdown voltage whereas at open channel, we see impact ionization current. At  $V_{\text{DS}}=4.5\text{V}$ , it reached  $5\mu\text{A/mm}$ . It is the first time that such a figure is obtained in this kind of device. The devices cannot be biased above  $4.5\text{V}$  without main risk of irreversible damage. Therefore, devices present small impact ionization current before degradation which is attributed to a large  $\Delta E_v$  of structure which prevents holes generated by impact ionization from flowing through the gate. This implies that these currents can hardly be observed when the Schottky diode is leaky. This explains that no similar experimental results has ever been published. Figure 6 show the gate current characteristic at  $V_{\text{DS}}=3.5\text{V}$  and measurements at X-band on a load-pull power set-up were performed. Output power increases with the gate-to-drain extension with a

maximum gain of 19dB. Concerning power saturation, we have remarked that the larger is the extension, the higher is the saturation power (40mW/mm for a narrow extension and 110mW/mm for a large extension). We explain this result as following : the further is the drain pad, the broader is the electric field distribution in the gate drain region. For a given drain voltage, the electric field peaks drops at the edge of the recess beside drain as the gate drain extension increases. This implies lower gate current. In addition, the high power of large extension devices can be attributed to a better excursion of the signal compared to a narrow extension device. The devices have been measured with the same bias conditions. In large extension devices, the gate current remains lower. At  $V_{DS}=3.5V$ , the maximum gate current reaches at open channel 800nA for a narrow extension and only 10nA for a large extension. Therefore, higher instantaneous drain voltage can be applied at the output which allows a larger excursion of the devices characteristics before impact ionization occurs. A recent result is performed. At  $V_{DS}=2V$  and  $V_{GS}=0.3V$ , with the large extension, thick cap devices have presented 140mW/mm and only 100mW/mm for thin cap devices.

Our result strongly suggests that the topology's optimization should improve output power. Thin cap layer devices exhibit high drain current, good Schottky diode breakdown voltage and lower gate current and it is clearly shown that larger extension implies lower gate ionization current.

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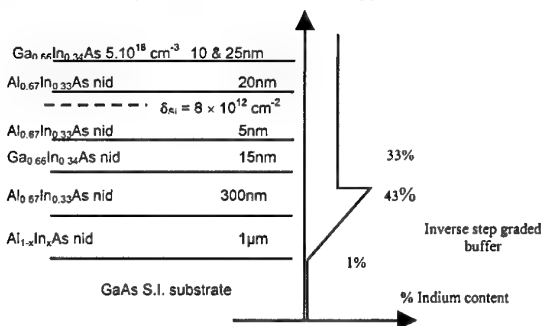


Figure 1 : Schematic of Simple Heterostructure-HEMT on GaAs substrate with the Indium composition profile

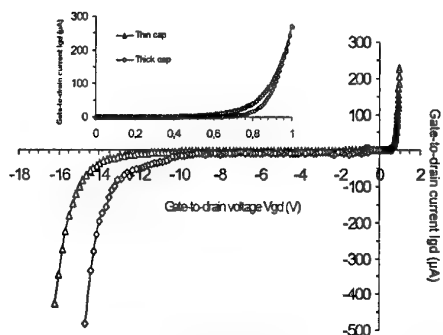


Figure 3 : Schottky characteristic for different cap layer thickness.

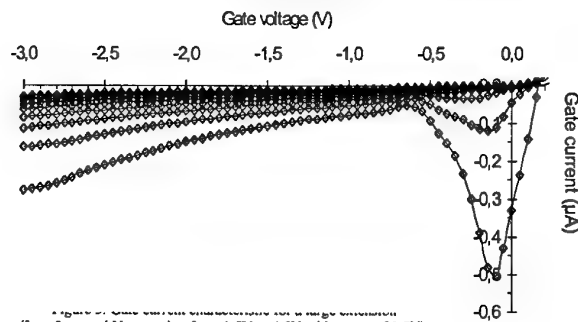


Figure 5 : Gate current characteristics for large extension ( $L_{SD}=3\mu m$  and  $V_{DS}$  varying from 1.5V to 4.5V with a step of 0.5V).

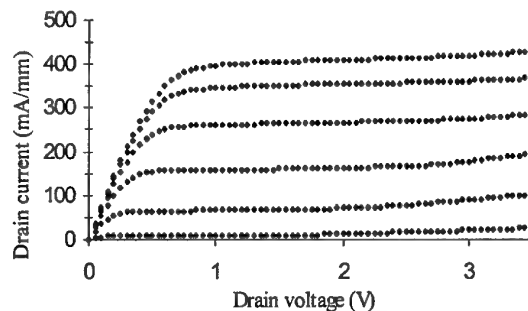


Figure 2: DC I-V characteristic of a Enhancement-mode metamorphic-HEMT with a gate of 0.4x100μm (Gate voltage maximum is +0.8V and gate voltage step size is 0.2V)

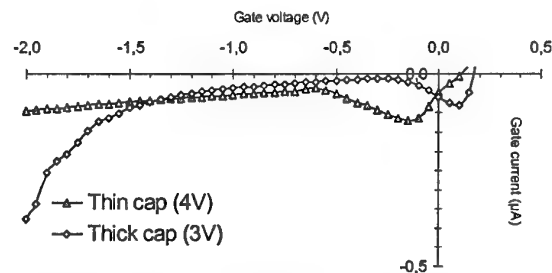


Figure 4 : Gate current for different cap layer thickness for large extension ( $L_{SD}=3\mu m$ ).

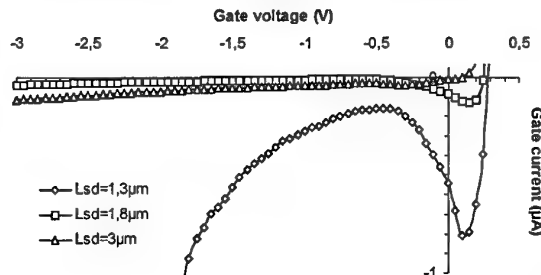


Figure 6 : Gate current versus gate voltage for different source to drain extension  $L_{SD}$ .

# Hybrid integration of thinned metamorphic HEMTs on Germanium

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## Abstract

*In this paper we first briefly discuss the performance of the devices grown on Germanium substrates. Further, we present a new technique for the hybrid integration of thinned MHEMTs and we show that the RF performance can be improved dramatically by removing the Germanium substrate.*

## Introduction

The increasing usage of MMICs in application fields such as the automotive industry is a strong driving force to develop alternative technologies with equal performance but lower cost. Here we report for the first time the successful hybrid integration of thinned metamorphic HEMTs (MHEMTs) on Germanium in a Multi-Chip Module with Dielectric layers (MCM-D). MCM-D is a special multi-layered thin film interconnection technology, used for high density packaging, consisting of a glass substrate (wafer) with alternating dielectric and metal layers on top. The integration of thinned individual HEMTs with passive circuitry on these substrates can result in low-cost advanced hybrid systems for mass-market millimeter wave applications.

## Methods and Results

As reported previously [1], high performant MHEMTs can be fabricated on Ge substrates. It has been demonstrated that these devices display DC performance parameters, comparable to MHEMT structures on GaAs, and even LM HEMTs on InP.

When comparing the HF performance of 0.2  $\mu\text{m}$  gate length devices to the GaAs based ones, a large discrepancy has been revealed, as is shown in Table 1. The dramatic drop in HF performance can be attributed to the limited resistance of the Ge substrate. Removal of the conductive substrate is the most feasible solution for this problem.

Before removal of the Ge substrate, the wafer is diced. Then a chip is mounted on a glass substrate (active side facing the glass) in a 3  $\mu\text{m}$  thick polymer layer (BCB). The frontside of the chip is now protected by the BCB. Hence, this dielectric layer is used as glue, in contrast to [1], where wax is used as glue. Removal of the Ge can be done by Reactive Ion Etching in a mixture of  $\text{CF}_4$  and  $\text{O}_2$ . Main advantage of this plasma method is the high selectivity of Ge towards GaAs, being the first epitaxial layer on top of the substrate.

The GaAs buffer can be removed selectively in a sulfuric acid based solution. As a final processing step, the buffer has to be removed outside the active region. A lithography step has to be performed and a non-selective etchant based on phosphoric acid is used. After this step, the metal contacts of these very thin devices (2  $\mu\text{m}$ ) are revealed and can be contacted by probe needles from the backside. Moreover, to be able to integrate these transistors in MCM-D substrates, their thickness has to be less than 5  $\mu\text{m}$  to circumvent planarization problems in subsequent MCM-D processing steps. So, substrate removal is also the solution for this problem. Figure 1 and Figure 4 show a schematical cross-section and a photograph of a thinned MHEMT on an MCM-D substrate.

Measurements done on these glass (MCM-D) wafers reveal a slightly reduced DC performance, as shown in Figures 2 and 3, but the RF performance recovers and is almost as good as for GaAs devices ( $f_T = 70 \text{ GHz}$ ,  $f_{\text{max}} = 120 \text{ GHz}$ ).

## Conclusions

To yield way to integration of Ge MHEMTs in low-cost MCM-D substrates, a highly selective method for substrate removal is presented. Combined with the low environmental load of this method, the presented process provides with a high performance technology ready for advanced hybrid integration.

## Reference

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Table 1. Overview of extrinsic HF characteristics for 0.2  $\mu\text{m}$  MHEMT devices, fabricated on the three types of substrates.

	GaAs based	Ge based (with substrate)	Ge based (substrate removed)
$f_T$ [GHz]	90	45	70
$f_{\text{max}}$ [GHz]	130	68	120

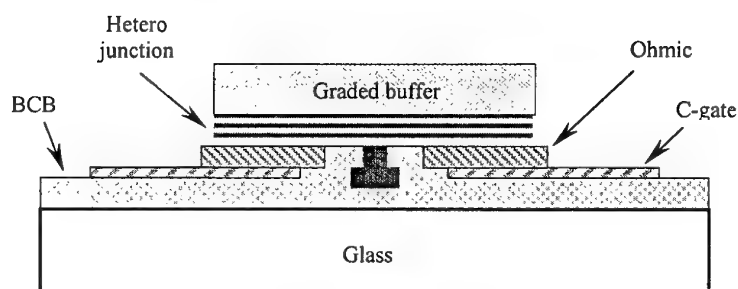


Fig. 1. Schematic cross-section of a thinned MHEMT glue mounted in a BCB layer on a glass MCM-D substrate.

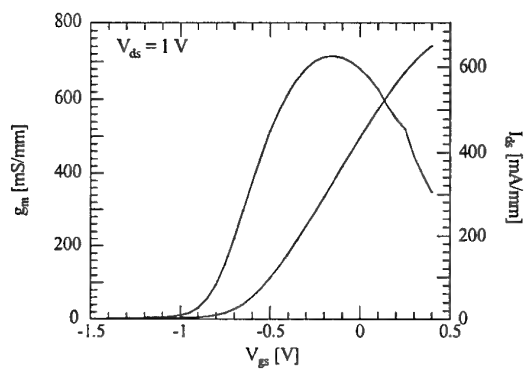


Fig. 2. Channel current and transconductance for 100  $\mu\text{m}$  wide MHEMT on Ge (without substrate removal)

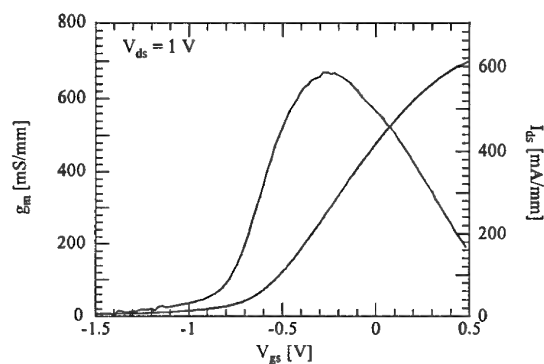


Fig. 3. Channel current and transconductance for 100  $\mu\text{m}$  wide MHEMT on Ge (after substrate removal)

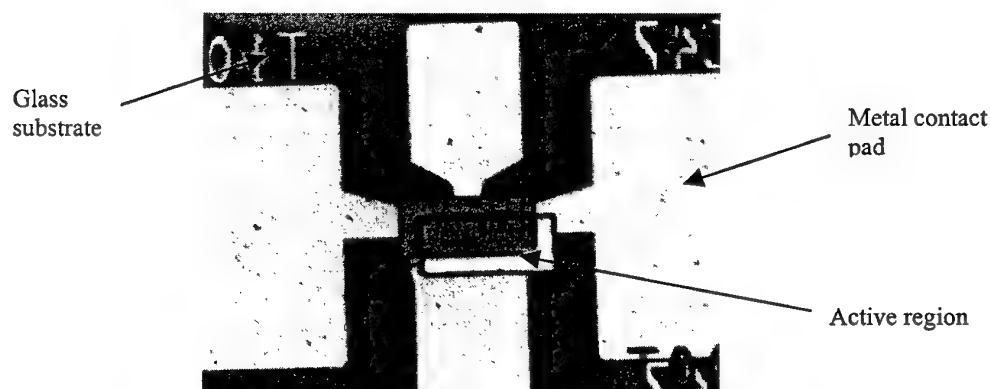


Fig. 4. Thinned MHEMT glue mounted in BCB on glass MCM-D substrate. (Notice the lithography misalignment for etching the buffer outside the active region.)

## Pseudomorphic InGaAs/InAlAs/InP-HEMTs for Cryogenic Applications

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InGaAs/InAlAs high electron mobility transistors are believed to be capable of playing an important role in various future communication systems due to their outstanding high-frequency and low noise performance (e.g. [1]). In this work the low temperature behaviour of first fabricated  $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  HEMTs is examined. This type of transistor is intended for working in low-noise cryogenic oscillators.

The HEMT layer system grown by MBE consists of a 15nm two-layer channel (7nm lattice-matched, 8nm pseudomorphic InGaAs) above a 200nm InAlAs buffer on InP, 5 nm spacer, 4 nm supply layer ( $n_{\text{Si}} = 3 \cdot 10^{18} \text{cm}^{-3}$ ,  $n_{\text{d, Si}} = 3.9 \cdot 10^{12} \text{cm}^{-2}$ ) and a 30nm barrier layer capped by Si-doped InGaAs. Hall measurements showed low field 2DEG-mobilities of more than  $11,000 \text{cm}^2/\text{Vs}$  and sheet carrier concentrations  $> 2.5 \cdot 10^{12} \text{cm}^{-2}$  at room temperature.

The quality of the ohmic contacts to the 2DEG quantum-well turned out to be one of the most critical parameters regarding extrinsic device behaviour. High source series resistances impair dc, high-frequency and noise performance. Temperature dependent transmission line model measurements revealed that the resistance of the alloyed Ni/AuGe/Ni contacts increases linearly with decreasing temperature (about  $0.01 \Omega \text{mm}/10\text{K}$ ). At the same time, the sheet resistance improves as expected since according to Hall measurements the low-field mobility increases while the sheet carrier concentration stays nearly constant (Fig. 1).

As a consequence, the drain current is reduced at cryogenic temperatures (Fig. 2). This reduction does not necessarily imply a decrease of the maximum extrinsic transconductance, as shown in Fig. 3. For a better comprehension of the HEMT behaviour a charge control model ( $n_s(x) \propto V_{\text{GS}} - V_{\text{T}} - V(x)$ ) [2] taking into account carrier velocity saturation and parasitic series resistances is used which is in acceptable agreement with the measured data. The saturation velocity is estimated from the high frequency measurements. 330nm gate length HEMTs exhibit a cutoff frequency  $f_t = 110\text{GHz}$  at room temperature (Fig. 4), while the maximum frequency of oscillation  $f_{\text{max}}$  is limited to 130GHz due to high series resistances.

Low temperature high frequency measurements are in progress. Test samples with a conductive, non-depleted cap layer showed lower contact resistance values and dependence on temperature. Detailed analysis will be given at the presentation.

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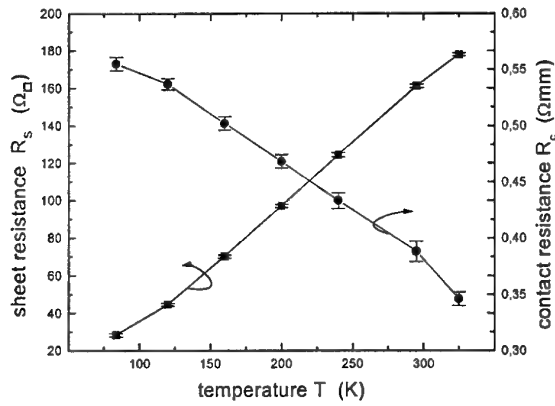


Fig. 1: Sheet and contact resistance dependence on sample temperature

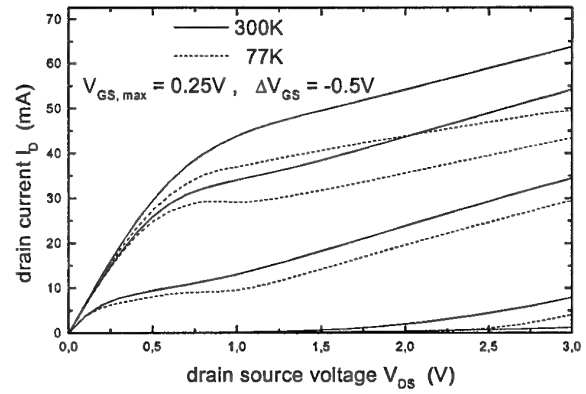


Fig. 2: HEMT output characteristics at 300K and 77K ( $w_g = 100\mu\text{m}$ ,  $l_g = 430\text{nm}$ )

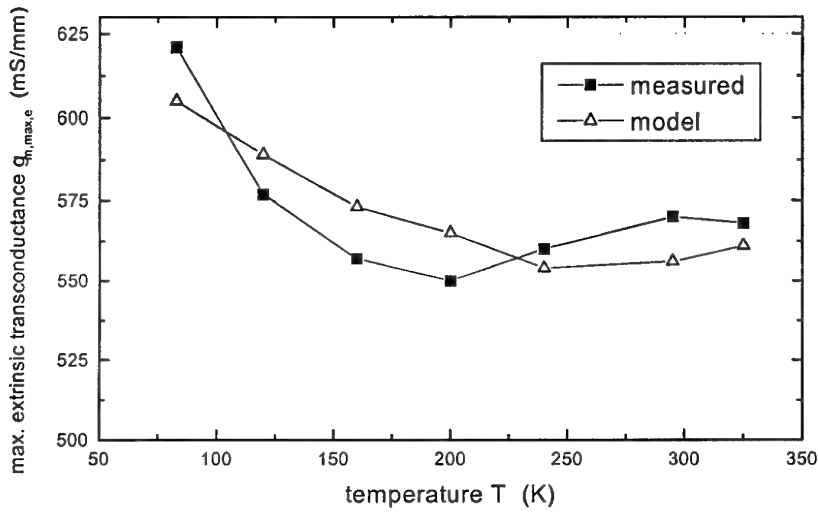


Fig. 3: Measured and modeled maximum extrinsic transconductances of a 330nm- $l_g$  HEMT at different temperatures

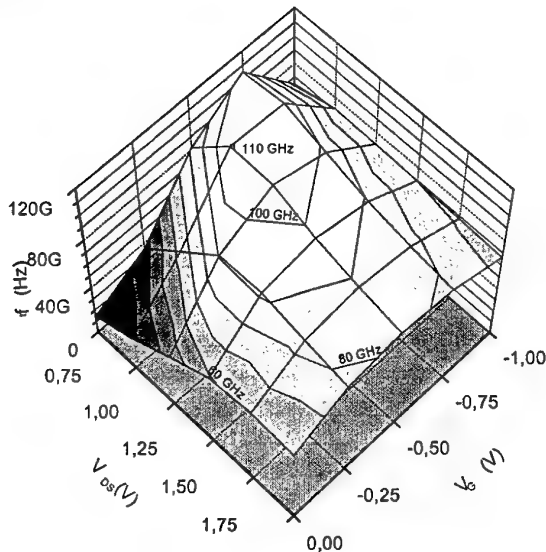


Fig. 4: Room temperature cutoff frequency  $f_t$  of a 330nm- $l_g$  HEMT at different bias points

# Optimization of AlGaAs/AlAs/GaAs quantum well infrared detector structures

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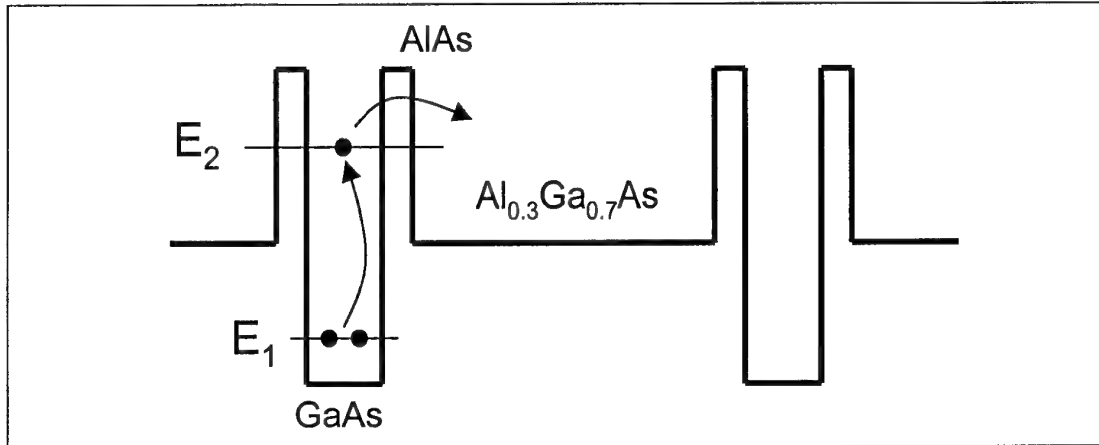
**Abstract.** Recently, quantum well infrared photodetectors have been used in focal plane arrays (FPA's) for imaging sensor systems [1]. The mature epitaxial growth and processing technology of GaAs leads to high uniformity, excellent reproducibility and accurate control of the band structure. This fact allows to fabricate monolithically integrated multiple spectral infrared detectors as well as their integration with high speed GaAs multiplexers and other electronics. Photodetectors operating in the 3-5  $\mu\text{m}$  regime are of technical interest due to the presence in the atmosphere of a transmission window at the mentioned wavelengths. These detectors exploited various absorption processes including miniband transitions in multiple quantum well (MQW) stacks, or bound-to-quasi continuum state transitions in GaAs/AlAs/Al<sub>0.3</sub>Ga<sub>0.7</sub>As superlattices [2][3]. In these latter devices, the electrons in Si-doped quantum wells are optically promoted to an excited state. Thin AlAs barriers at both sides of the well allow the carriers to tunnel out into the Al<sub>0.3</sub>Ga<sub>0.7</sub>As transport layers instead of relaxing to the quantum well ground state (see fig. 1).

In this work, we focused on the special contribution of the AlAs thin tunnel barriers in the performance of a GaAs/AlAs/Al<sub>0.3</sub>Ga<sub>0.7</sub>As quantum well infrared detector. First simulation studies were performed to estimate an initial value for the width of these layers. With those calculated values, an important experimental work was carried out in order to optimize the responsivity of the device. The samples, grown by Molecular Beam Epitaxy, were processed into multiple internal reflection waveguide and "mesa" etched photodetectors, and then characterized by Fourier Transform Infrared Spectroscopy and responsivity measurements. A direct relationship between the AlAs tunnel barrier width and the responsivity of the device has been observed (see fig. 2). In addition, different growth procedures were studied to improve the quality of the AlAs/Al<sub>0.3</sub>Ga<sub>0.7</sub>As interfaces.

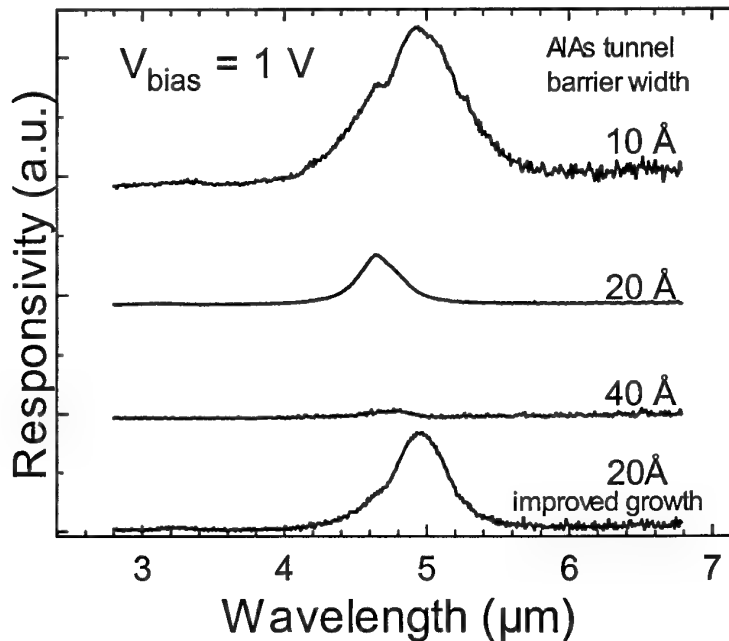
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**Fig 1.** Conduction band potential profile for a 3-5  $\mu\text{m}$ , GaAs/AlAs/AlGaAs quantum well infrared photodetector, showing the carrier absorption and escape mechanism.



**Fig 2.** Responsivity measurements for samples with different AlAs barrier width. A curve corresponding to a sample with improved interfaces is also presented.

## **Heterobarrier issues for AlInAs-GaInAs 1.5 $\mu$ m Lasers**

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Quantum well lasers are recognised as one of the key requirements to satisfy the increasing demands of fibre optic networks, optical interconnects and optical information storage systems. These applications require low threshold current densities and associated low temperature sensitivity. Though the operation of these devices is now understood, it is also recognised that the strained layer multiquantum well devices suffer from internal carrier transport effects with degraded internal quantum efficiency and reduced high speed modulation performance.

The carrier transport effect is seen by the leakage of carriers from the wells as a result of limited well barrier height. Narrow quantum wells, which determine the laser wavelength, require thick optical confinement layers of limited barrier height, i.e. smaller than the cladding region, which gives rise to a restriction of the barrier bandgap. The thickness of the confinement region then imposes enhanced delay times.

A method to artificially increase the heterobarrier involves the insertion of a multiquantum barrier layer in the waveguide region, and has been successfully demonstrated for short wavelength laser diodes. The multiquantum barrier enables the feedback of electrons from the wells through the artificially enhanced barrier and at the same time maintains a constant refractive index for the confining layers.

In this paper we study the effect of the barrier height on current transport by loading an AlInAs-GaInAs multiquantum barrier for the InP system, for long wavelength lasers. Some preliminary results are presented through transport measurements and suggestions made to improve carrier injection to avoid carrier transport effects.

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